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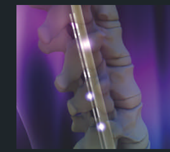

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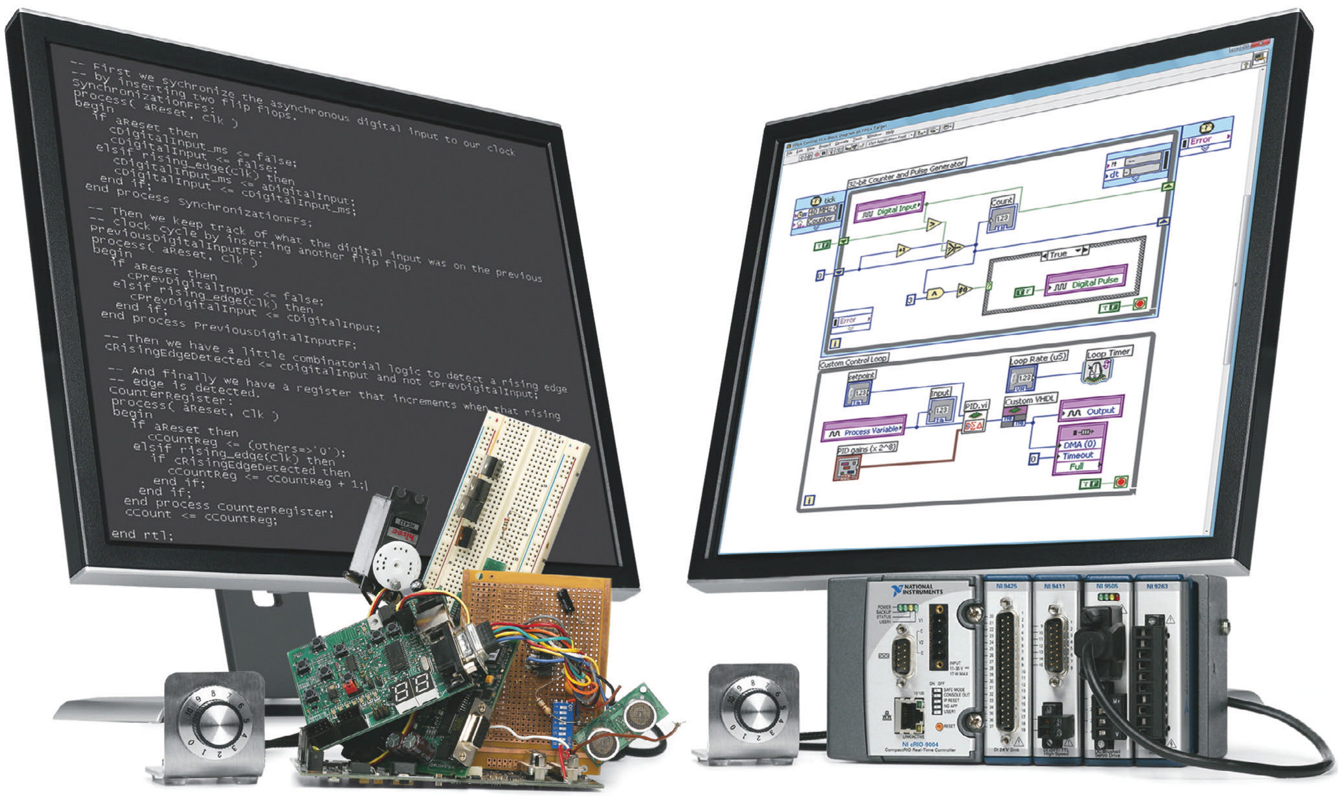

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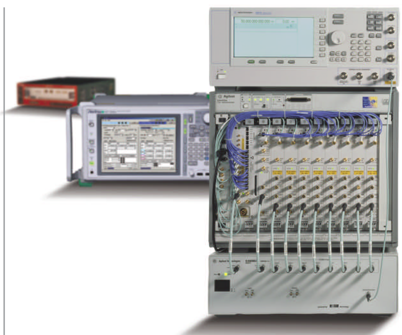
Power fortunes: estimating power in FPGA designs



40- and 100-Gbps Ethernet brings new test challenges

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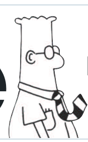
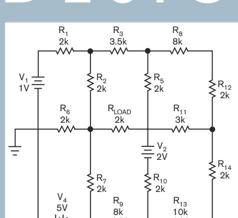


Use alternative approaches to evaluate dc/dc synchronous buck converters

DESIGNIDEAS



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DEPARTMENTS & COLUMNS

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ONLINE ONLY

Check out these Web-exclusive articles:

Establishing timing correlation between tools

It is vital to a smooth IC-design flow that the various tools in the flow agree in their timing analysis.

→www.edn.com/article/CA6644807

Multicore programming: easy or difficult?

Many commentators are concerned that efficiently and correctly porting code onto platforms with four or more cores is beyond the capabilities of many engineers. Others simply state that this problem is solved and that currently available mature SMP operating systems and threading libraries are well-understood.

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News and New Products

LabView 8.6 adds wireless, enhances multicore and FPGA features

By Martin Rowe, Test & Measurement World -- EDN, 9/18/2008

National Instruments continues to expand the horizons for LabView, its popular graphical programming language. With the introduction of Version 8.6, LabView can now control the company's wireless data-acquisition products, and the software also extends beyond its traditional test-and-measurement base into multicore processing and embedded-system design. LabView 8.6 lets you make remote measurements using a Wi-Fi connection to data-acquisition devices. You can connect to wireless devices through technologies such as Bluetooth, GPRS (general packet-radio service), and GSM (global-system-for-mobile) communications.

LabView 8.6 software provides multicore-optimized analysis and signal-processing functions to increase the performance of automated-test systems, such as wireless-device testers.

Using these technologies, you can develop a wireless-sensor network and control it with LabView. You can also download drivers for numerous proprietary wireless-sensor networks, and, using the LabView Wireless Toolkit, you can test wireless devices that use any of these technologies.

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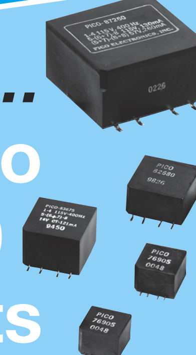

BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

Canceling Sirius: so frustrating, it made me furious

Tough economic times understandably encourage subscription-service companies to do their utmost to hold onto customers. Sometimes, they achieve this goal by making the service too tempting to discard, offering free months, free extras, and other perks. And sometimes, unfortunately, they achieve this goal by making the cancellation too difficult to accomplish. America Online (www.aol.com), for example, has gotten into plenty of legal trouble in recent years for such despicable behavior. And, if my experience and that of other frustrated online activists indicates a general trend, beleaguered Sirius Satellite Radio (www.sirius.com) is due for some regulatory attention, too.

I've been a Sirius subscriber since October 2004, but I've never listened to the service much in my car, in no small part because, as a home-based worker, I don't have a daily office commute. Conversely, I've made regular use of the Sirius Online streaming music service, specifically the 32-kbps configuration that comes with my subscription. However, in February, I received an e-mail warning me that free online access would end by March 11 if I didn't "renew now," even though my subscription was active through later that month. Whenever I launched the Sirius Online player, pop-up windows would echo that warning, indicating that, unless I renewed early—for a one-, two-, or three-year term—my only streaming option after March 11 would be an incremental-cost, albeit higher-bit-rate, service variant.

Frankly, I've been listening to Sirius Online less and less with the passage of time. I've got a formidable library of network-stored music ripped from CDs. My Microsoft (www.microsoft.com) Zune subscription-music service, which includes 128 streamed channels, provides additional music content. Plenty of other low-cost or free online streamed-music sources, such as Pandora (www.pandora.com), are also available. And I have little confidence that Sirius will still be a viable business entity a year from now, much less two or three years. So, I decided to cancel my Sirius service before the cutoff date.

While trying to perform what should have been a simple task, I encountered several annoying barriers. First, Sirius provided no online or e-mail option for service cancellation or, for that matter, even automatic-renewal cancellation. The only way to cancel is to contact customer service by the phone number the company publishes on its Web site. When I tried that option, I encountered a Byzantine automated-menu system and lengthy hold delays followed by hang-ups. After my second disconnection experience, I checked out a discussion thread at SiriusBuzz.com (http://siriusbuzz.com/forum/showthread.php?t=228). From that experience, I learned that, even if I had gotten through to a human, that person would have told me to dial a different, unpublished number dedicated to cancellation requests. So, for my third cancel-by-phone attempt, I tried this alternative number instead.

After yet another wait of more than a half-hour, I reached someone. However, after providing my name, phone number, mailing address, and e-mail address and after firmly and repeatedly stating that I wanted to cancel my service, the person on the line, having repeatedly tried to persuade me otherwise, put me on hold. In 10 minutes, another person got on the phone. Again, I provided my name, phone number, mailing address, and e-mail address. This person again asked me several times if I was sure I wanted to cancel my service. Eventually, the cancellation went through, but it would not become effective for more than two weeks. The customer-support person claimed that she couldn't process an early-termination request. Though I doubted her sincerity, I decided against enduring even more delay and frustration just for a two-plus-weeks'-worth credit on my bill.

The experience bolsters my conviction that Sirius is in a fiscal last-gasp situation. Even though other folks in my shoes might have given up, thereby allowing Sirius to retain subscribers in the short term, the company's behavior will do only further harm to its long-term viability. It reminds me of those Internet companies that sign up my e-mail address for newsletters, promotional messages, and the like and then refuse to honor my requests to unsubscribe. But when the short term looks so grim, I guess Sirius doesn't have the luxury of caring about the long term. Caveat emptor, folks. EDN

Contact me at bdipert@edn.com.

+ Read more on this topic at www.edn.com/090423eda.

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Buck regulators with integrated MOSFETs simplify designs up to 25A/phase

High efficiency

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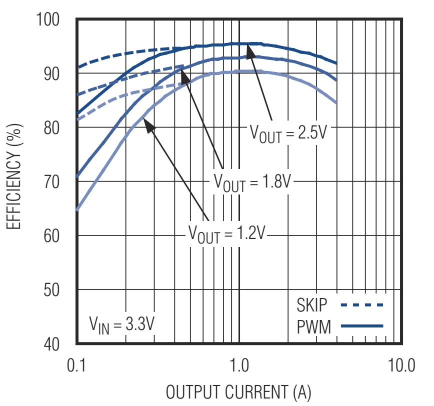

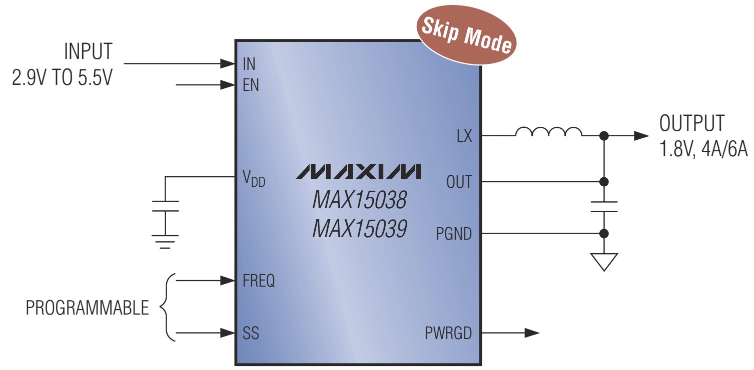

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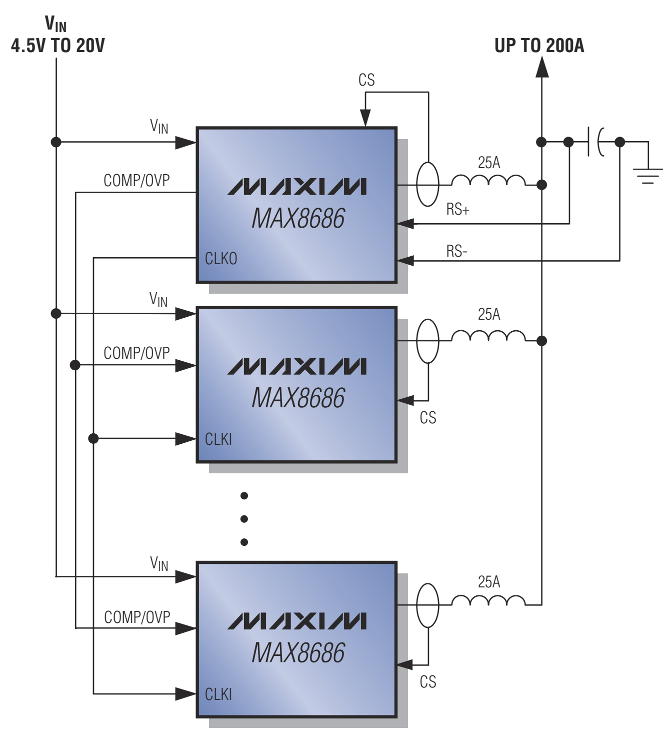
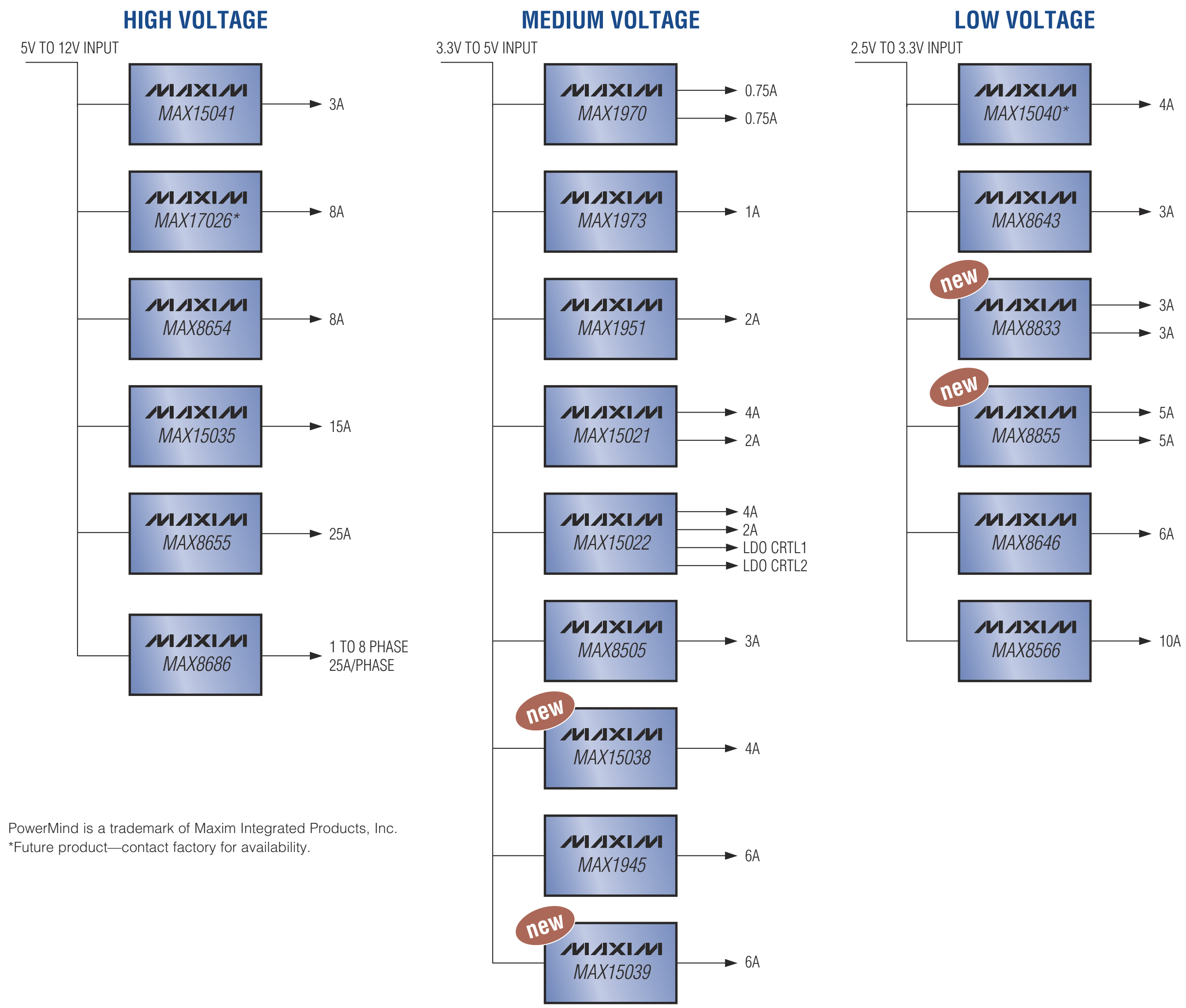


Maxim's PowerMind™ family of integrated buck regulators simplifies your toughest design challenges. These regulators provide high efficiency in compact, simple, cost-effective solutions that have the industry's lowest EMI.



PowerMind is a trademark of Maxim Integrated Products, Inc.
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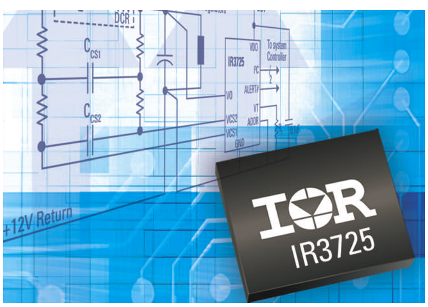
EDITED BY FRAN GRANVILLE

pulse

INNOVATIONS & INNOVATORS

IC monitors input power

International Rectifier has introduced the IR3725 input-power-monitoring IC. The device communicates with a host system over the I²C (inter-integrated-circuit) bus to monitor input power, voltage, and current for power supplies operating on 8 to 23.5V inputs. Current-monitoring accuracy is 1%, and voltage-monitoring accuracy is 1.5%. Worst-case power-measurement error is 2% over the full temperature range and 1.5% over a 0 to 85°C range. A PSI (power-state-indicator) interface provides the ability to maximize efficiency at light loads. The IC operates from a 3.3V bus, and you can set up a programmable open-drain-alert pin to indicate when power exceeds a programmable level.



The IR3725 IC monitors voltage, current, and power for buck regulators operating from a 12V input.

The device can use a discrete current-sensing resistor or the DCR (dc resistance) of the power inductor in the buck regulator it is monitoring. It includes an internal thermal-compensation circuit that accounts for the varying DCR of the power inductor. You can program the averaging interval of the measurement through the I²C bus.

The IR3725 provides input power monitoring for energy-efficient CPU, server, and storage applications. It comes in a 12-pin DFN package, operates in the −10 to +150°C temperature range, and sells for $1.25 (10,000).

—by Paul Rako

▷**International Rectifier**, www.irf.com.

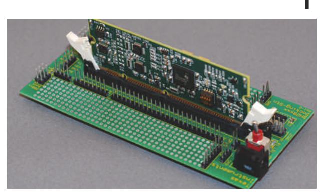
FEEDBACK LOOP

"A CFL (compact-fluorescent-lighting) blog ... normally generates lots of response, but this one is so comprehensive that it's mostly produced a stunned silence—a fine reference point in a sea of BS, misinformation, and plain lies."

—Reader Darren Holdstock, in *EDN*'s Feedback Loop, at www.edn.article/CA6632368. Add your comments.

Floating-point microcontroller doubles performance

Targeting the needs of high-performance applications, Texas Instruments' TMS320C2834x Delfino controllers offer twice the floating-point performance of previous TMS320C2000 devices. The C28x core operates at 300 MHz; surrounding the core on-chip are 516 kbytes of single-cycle access RAM; a single-precision, 32-bit floating-point unit; and 65-psec-resolution PWM (pulse-width-modulation) modules. Communication peripherals include CAN (controller-area-network), I²C (inter-integrated-circuit), SPI (serial-peripheral-interface), and SCI (serial-communication-interface) controllers. The controller includes an external ADC interface with interrupt-trigger support.


Modular control-card daughtercards provide development support for Delfino devices. The daughtercards plug into TI's evaluation and application boards.

Two Delfino microcontrollers are now available for sampling. The TMX320C28346 superset configuration is available for prices starting at $19.70 (100). The smaller TMX320C28343 operates at 200 MHz, includes 260 kbytes of on-chip RAM, and is available for prices starting at $13.50 (100). Two modular control-card daughtercards provide development support for these devices. The daughtercards plug into TI's evaluation and application boards, such as the renewable-energy, resonant-dc/dc, and peripheral-explorer developer's kits. The C28346 DIM168 (TMDXDOCK28346-168) and the C28343 DIM100 (TMDXDOCK28343) experimenter's kits are also available for $189 and $159, respectively.**—by Robert Cravotta**

▷**Texas Instruments**, www.ti.com.

Customizable microcontroller, $75,000 NRE costs target 10,000-unit applications

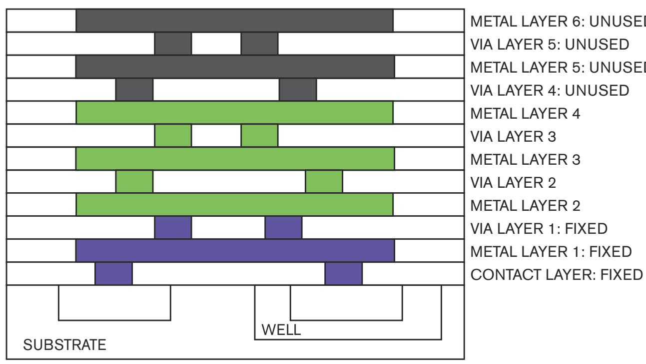
Atmel's AT91CAP7L standard-product microcontroller has as many as 200,000 gates of MCPF (metal-programmable-cell fabric) that you can use to implement proprietary customer IP (intellectual property), hardware accelerators, additional processor cores, or peripherals. The CAP7L relies on the company's second-generation MPCF-II technology to reduce to $75,000 the NRE (nonrecurring-engineering) costs of implementing 200,000 gates of proprietary custom IP with an ARM7 (www.arm.com) core. For applications that target as few as 10,000 units, this combination results in a fully amortized unit cost of $18, including NRE costs and IP licensing.

The original MPCF technology, which Atmel announced in 2007, uses six metal layers and five via layers for the MP (metal-programmable)-library-cell configuration and interconnect. The new MPCF-II technology uses a new via-programmable-cell library that trades density for cost and supports configuration and routing of the chip using three metal layers and three via layers. This approach reduces the number of masks you need to modify from 12 with the first-generation MPCF to six with the new version and cuts the NRE costs by 50%.

Prototypes are available within 10 weeks of receiving the final gate-level netlist, and production quantities are available within 12 weeks. CAP7E microcontrollers with built-in FPGA interface are available now for $9.50 (10,000), and CAP7L customizable microcontrollers are available now for $5.50 (50,000).

The MP block comprises about 15% of the CAP7L die area. The remaining 85% of the die is predefined, consisting of an ARM7 core with a four-layer AHB (advanced high-performance bus) and 22-channel peripheral-DMA controller; a USB (universal-serial-bus) device; an SPI (serial-peripheral-interface) master and slave; two USARTs; three 16-bit timer/counters; an eight-channel, 10-bit ADC; 160 kbytes of SRAM; and a system controller, including interrupt, power-control, and supervisory functions. The MP block sports two AHB masters and two AHB slaves, 14 APB (advanced-peripheral-bus) slaves, and 32-bit programmable I/O that you can hardware-select to share I/O. An on-chip priority-interrupt controller provides as many as 13 encoded interrupts and two additional unencoded interrupts for DMA transfers.

You initially develop the design using an Altera (www.altera.com) or Xilinx (www.xilinx.com) FPGA and an ARM7 microcontroller. You develop the HDL (hardware-description-language) code for any custom IP using standard, vendor-specific or third-party FPGA-design tools. Once it verifies the design, Atmel needs only the RTL (register-transfer-level) netlist to implement in the MP block on the CAP7L.



MPCF-II trades density for cost, using three metal layers and three via layers–down from 12 layers for the first-generation MPCF implementations.

Atmel provides the CAP7E ARM7-based microcontroller with direct FPGA interfaces. The interface on the CAP7E affords the FPGA direct access to the AHB and peripheral-DMA controller on the CAP7L. Atmel also provides FPGA logic that decodes and encodes the bus traffic that flows between the FPGA and the CAP7E microcontroller. The logic blocks in the FPGA connect to the CAP7E through the AHB-master and -slave channels. You use the CAP7E-plus-FPGA implementation for early market testing and proof of concept before migrating to the CAP7L.

Atmel also provides a library of license- and royalty-free IP that the company has fully verified and tested in the CAP7L MP block. The IP includes a USART supporting RS-232, RS-485, ISO 7816, and IRDA (Infrared Data Assocation) standards; an SSC (serial-synchronous controller); TDM (time-domain multiplexing); I^2S (inter-IC sound); an AC (audio codec) 97 controller; component specification Version 23; two-wire master and slave interfaces; an SPI; an SD (secure-digital)-card/MMC (multimedia-card) host controller; and others. For the full list of supported interfaces, go to www.edn.com/090423pa.

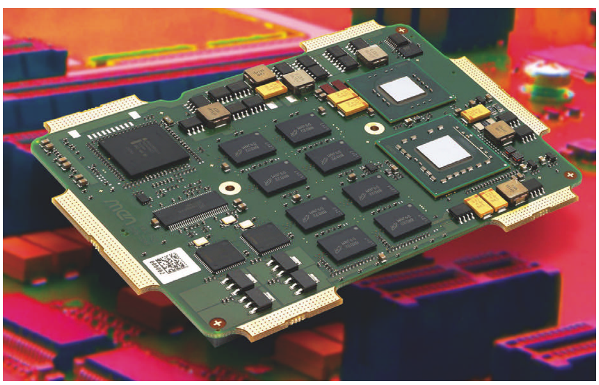
—by Robert Cravotta

▷**Atmel**, www.atmel.com.

DILBERT By Scott Adams

Rugged system on module supports fabric interconnects

As embedded-system designers confront the latest transportation, avionics, industrial-automation, and medical-instrumentation applications, the main challenges are to deliver a system that meets high-performance and low-power requirements and that can survive in a hostile environment. MEN Micro simplifies this task with its latest generation of ESMexpress (embedded-system-module express) SOM (system-on-module) products, which it based on the Intel (www.intel.com) Core 2 Duo SP9300 processor with a clock frequency as high as 2.26 GHz. The XM2 comes with the Intel GS45 graphics controller, which provides a 16-lane PCIe (peripheral-component-interconnect-express) graphics link or as many as two SDVO (serial-digital-video-out) interfaces, a DisplayPort, or two HDMI (high-definition-multimedia-interface) ports.



MEN Micro based its latest generation of ESMexpress SOM products on the Intel Core 2 Duo SP9300 processor with a clock frequency as high as 2.26 GHz.

The new Core 2 Duo-based module also features a host of I/O functions, including four one-lane or one four-lane PCIe link and two GbE (gigabit-Ethernet) ports, eight USB (universal-serial-bus) ports, three serial ATA (advanced-technology-attachment) ports, and one high-definition-audio port. The XM2 dissipates as much as 40W through the fanless cooling system and provides 100% EMI (electromagnetic-interference) protection when you mount it to a frame and enclose it in an aluminum housing, as the ESMexpress standard specifies. A fixed pin assignment guarantees that ESMexpress modules remain interchangeable. Operating temperature for the XM2 is 0 to 60°C for both convection and conduction cooling. Prices for the XM2 ESMexpress module start at $1911.

> The XM2 dissipates as much as 40W and provides 100% EMI.

ESMexpress, which VITA (VMEbus International Trade Association, www.vita.com) is currently developing as ANSI (American National Standards Institute)-VITA 59, RSE (rugged system-on-module express), combines advanced cooling techniques, the latest serial buses, and rugged components with the SOM model.

—by Warren Webb

▷**MEN Micro**, www.menmicro.com.

CLOCK GENERATOR REFLECTS COMPLEXITY OF INTEL CALPELLA MOTHERBOARDS

SpectraLinear built its new SL28748 clock-generator IC to work on the Intel (www.intel.com) Calpella mobile platform. In doing so, SpectraLinear opens a window on an interesting comparison between the problem of generating and distributing clocks for a mobile, media-centric PC motherboard and doing clock-tree synthesis on an SOC (system on chip).

"In the board world, the PC motherboard is … unique because there are so many clock requirements," says SpectraLinear's vice president and business-unit manager, Elie Ayache.

For these devices, the clock-generator chip must be highly configurable. You need to avoid having a special power-up-and-configure cycle for the clock chip, and the bill-of-materials budget for a typical motherboard can't tolerate an additional programmable ROM just to initialize the clocks. So, the configuration information for the clock chip should be on the chip. SpectraLinear uses a large amount of OTP (one-time-programmable) memory that the company configures at the factory for customer orders, along with I²C (inter-integrated-circuit)-programmable registers for parameters that can change during operation. The result is a small die and a high degree of configurability.

And, because Calpella is a mobile platform, power management becomes an issue. The SpectraLinear design team attacked every aspect of power dissipation in the chip—from the core to the outputs. The 0.18-micron chip has its own multiple voltage regulators operating from the 3.3V input supply, allowing SpectraLinear to turn down the voltage to each voltage-controlled oscillator just until it locks at the required frequency.

Add to that the ability to adjust the output voltages down to 1.05V and to tune each I/O to its environment on the board, and you get as much as 50% power savings compared with alternative approaches, according to the company. The preliminary data sheet claims that the device has 100-mA dynamic current on the 3.3V supply under full load. For more on this chip, go to www.edn.com/090423pb.

—by Ron Wilson

▶**SpectraLinear, www.spectralinear.com.**

04.23.09

VOICES

Signal-integrity experts speak out

At DesignCon 2009, which took place in Santa Clara in February, *EDN* got a chance to talk about signal integrity with Greg Edlund and Larry Lerner, who presented a panel at the conference (**Reference 1**). Greg Edlund is a senior engineer in IBM's electronic-packaging and integration-technology department. He recently published a book on timing analysis and simulation for signal-integrity engineers (**Reference 2**). Larry Lerner is a senior R&D manager at Agilent Technologies' EEsof division, where he is responsible for EEsof's product development and signal-integrity strategy. For an expanded version of this interview, as well as the reference list, go to www.edn.com/090423pc.

What do you mean by "signal integrity?"

A **(Edlund)** In the most general sense, signal integrity is the branch of engineering having to do with the reliable transfer of data between two chips. By necessity, it also encompasses chip-to-chip timing and power-distribution networks.

Is signal integrity a big problem, and is it specific to your area of design?

A **(Lerner)** If you like fast computers and fast downloads, you should care about signal integrity. Computer, data-center, and telecom equipment contains tens or hundreds of chips that have to communicate with each other with multigigabit-per-second data rates and a low bit-error rate. Preserving signal integrity is a challenge because, at today's data rates, [you must mitigate] electromagnetic impairments previously only seen in the microwave-frequency range. Attenuation, reflections, and crosstalk must be countered by prelayout- and post-layout-design optimization and by introducing new techniques, such as impedance matching, pre-emphasis, and equalization. Chip-to-chip connections are mini communication systems. It's a challenge wherever you have chips communicating at high speed.

What is the nastiest signal-integrity problem you have seen?

A **(Edlund)** Signal-integrity problems come in two flavors: those with a single dominant root cause and those with many small contributing factors of roughly equal size. Each kind can be equally devastating, but the second flavor is particularly difficult to diagnose because it involves in-depth knowledge of how much each factor contributes to the erosion of operating margin and how they interact with one another.

A **(Lerner)** We see two pinch points currently: For cost-driven consumer applications, the parallel buses,

Edlund Lerner

such as DDR, take the most space. It's tempting to compact them, but the risk is postlayout failure. To avoid re-spins, we're seeing a lot of predictive post-layout verification using EM [electromagnetic] simulators, such as [Agilent's] Momentum. For performance-driven applications, the pinch points are prelayout-design-space exploration and optimization of the serial links. In this case, we're using sophisticated signal processing to get the links to work at about 10 times the speed of DDR. But there are many parameters to tune: pre-emphasis, interconnect design, equalization. The tool for this task is [Agilent's] Channel Simulator. It's a two-step simulation with a Spice-like phase that first extracts an FIR [finite-impulse-response] model from the circuit using an impulse response and then runs bit patterns through the extracted model.

What is your company doing to solve signal-integrity problems?

A **(Lerner)** We help signal-integrity engineers be productive by offering a complete signal-integrity workflow—no more stringing point tools together with sealing wax, bailing wire, and PERL [Practical Extraction and Report Language] scripts.

What recommendations do you have for design engineers to avoid signal-integrity problems?

A **(Edlund)** Reach beyond models and simulations to understand the physics of failure. It is imperative for signal-integrity engineers to have a clear picture of how various failure mechanisms combine and the relative size of each contribution. This information is not easy to come by. It involves designing test hardware, using it to characterize components in the lab, and linking component behavior to system performance.

A **(Lerner)** Iterating the hardware to success isn't the answer. You need the insight and what-if capabilities of simulations—verified against measured prototypes, of course—to be first to market.

What do you see in the future for signal integrity?

A **(Edlund)** The electromagnetic behavior of interconnect systems is becoming more difficult to subdivide into independent components. Signal-integrity engineers need to understand how components interact with each other so they don't miss important effects by making the models too small. In the future, successful signal-integrity engineers will use 3-D field solvers in the same way they used Spice in the early days: to enhance their understanding of system behavior. This implies that the cost of 3-D field solvers needs to fall to make them accessible to more engineers.

A **(Lerner)** There's always a "more" to higher speed, but, in addition, the workflow must grow in capability to encompass not only signal integrity, but also power integrity, EMC [electromagnetic compatibility], and EMI [electromagnetic interference].

–Interview conducted and edited by Paul Rako

RAQ's

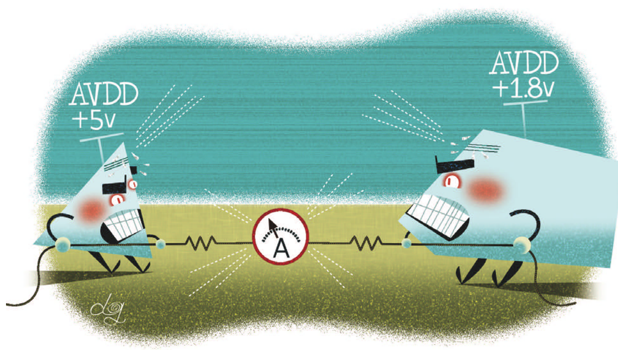
Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Keeping Common Modes Common

Q. How come my A/D converter is not able to achieve full scale as the datasheet specifies?

A. ADC datasheets specify a common-mode voltage requirement for the analog inputs. Not much detailed information is available on this subject, but the proper front-end bias must be maintained in order to achieve rated performance at full scale.



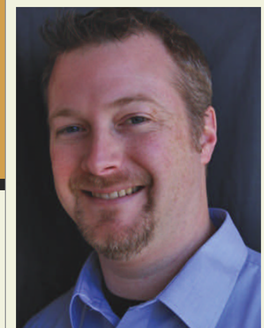
ADCs with integrated buffers typically have an internally biased common-mode level of half the supply plus a diode drop (AVDD/2+0.7V). No external circuitry is required to bias this circuit, but it must be maintained to properly use the converter. For un-buffered (e.g., switched-capacitor input) converters, the common-mode bias is typically half the analog supply, or AVDD/2. This can be supplied externally in a variety of ways. Some converters have a dedicated pin that allows the designer to provide bias through a couple of resistors tied to the analog inputs. Alternatively, the designer can connect the internal bias to a transformer's center tap, or can use a resistor divider off the analog supply (a resistor from each leg of the analog inputs to AVDD and ground). Check the manufacturer's datasheet or applications support group before using the VREF pin, as many references are not equipped to supply a common-mode bias without an external buffer.

If the common-mode bias is not provided or maintained, the converter will have gain and offset errors that contribute to the overall measurement. The converter may "clip" early, or not at all because its full scale cannot be reached. Common-mode bias is especially important when connecting an amplifier in front of the converter, especially if the application calls for dc coupling (required for sampling dc or very low frequency signals). Check the amplifier's datasheet specifications to make sure the amplifier can meet the converter's swing and common-mode supply requirements. Converters have been pushing to smaller geometry processes and therefore lower supplies. With a 1.8-V supply, a 0.9-V common-mode voltage is required by the amplifier. Amplifiers with 3.3-V to 5-V supply voltages may not be able to maintain that low a level, but newer low-voltage amplifiers can.

Overlooking a converter's common-mode input voltage specification can cause havoc in any design. If multiple stages are used, the common-mode levels must be kept the same to prevent the two components from "fighting" each other. One will usually win, producing bogus measurements. For ac-coupled applications, use a coupling capacitor between the two stages to break the common-mode mismatches. This allows the design to optimize the bias of both the amplifier output and the ADC input.

To Learn More About Common Mode Voltages

http://designnews.hotims.com/23101-101



Contributing Writer Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

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BY BONNIE BAKER

Where did all that racket come from?

Since arriving in the market, CMOS single-supply amplifiers have been beneficial to single-supply-system designers worldwide. Key players affecting the THD+N (total-harmonic-distortion-plus-noise) characteristics of dual-supply amplifiers are input noise and output-stage crossover distortion. The THD+N performance of a single-supply amplifier also originates in the amplifier's input and output stages. However, the input stage's impact on THD+N complicates the nature of this specification with single-supply amplifiers.

Several types of single-supply amplifier topologies can accept input signals across the power supplies. In the complementary-differential-input-stage topology, when the amplifier's inputs are near the negative rail, the PMOS transistors are on, and the NMOS transistors are off. When the amplifier's inputs are closer to the positive rail, the NMOS transistors are on, and the PMOS transistors are off. For an illustration of this topology, see www.edn.com/090423bb.

This design topology has significant variations in the amplifier's offset voltage across the common-mode input range. In the input region near ground, the PMOS transistor's offset error is dominant. In the region near the positive power supply, the NMOS-transistor pair dominates the offset error. Both pairs are on as the amplifier's inputs pass between these two regions. The end result is that the input offset voltage changes between the stages. When the PMOS and NMOS transistors are both on, the common-mode voltage region is approximately 400 mV. This crossover-distortion phenomenon affects the amplifier's THD. If you configure the complementary-input amplifier in a noninverting configuration, the input crossover distortion can affect the amplifier's THD+N performance. For instance, in **Figure 1** the THD+N is 0.0006% if you avoid using the input transition. If the THD+N tests include the amplifier's input crossover distortion, the THD+N is 0.004%. You can avoid this type of amplifier crossover distortion by using an inverting configuration.

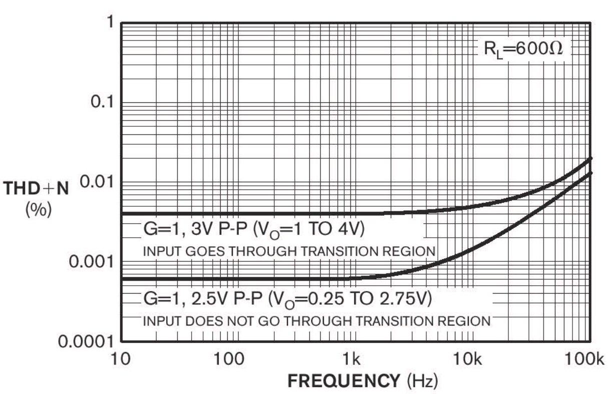

Figure 1 The THD+N is 0.0006% if you avoid using the input transition, or 0.004% if the THD+N tests include the amplifier's input crossover distortion.

Another major THD+N contributor can be the operational amplifier's output stage. The output stage of a single-supply amplifier usually has an AB topology. As the output signal sweeps from rail to rail, the output stage displays a crossover distortion similar to the input-stage crossover distortion, in that the output stage switches from transistor to transistor. Generally, a higher level of quiescent current through the output stage reduces the amplifier's THD. The amplifier's input noise is another contributor to the THD+N specification. A high level of input noise, high closed-loop gains, or both can increase the amplifier's overall THD+N level.

To optimize a complementary-input-single-supply amplifier's THD+N performance, place the amplifier in an inverting-gain configuration and keep the closed-loop gain low. If the system requires the amplifier to be configured as a noninverting buffer, an amplifier with a single-differential input stage and charge pump is a more appropriate choice. **EDN**

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Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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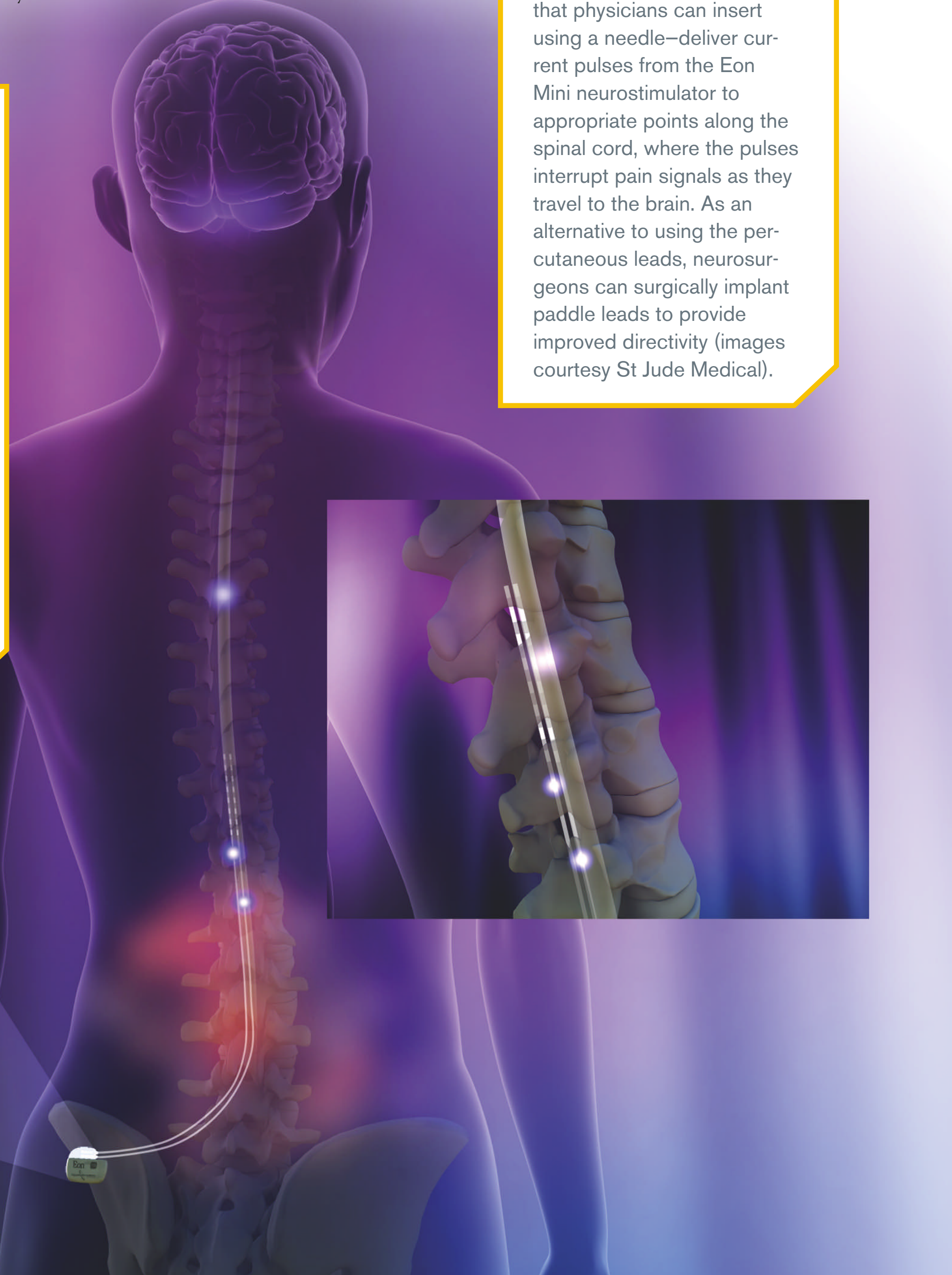
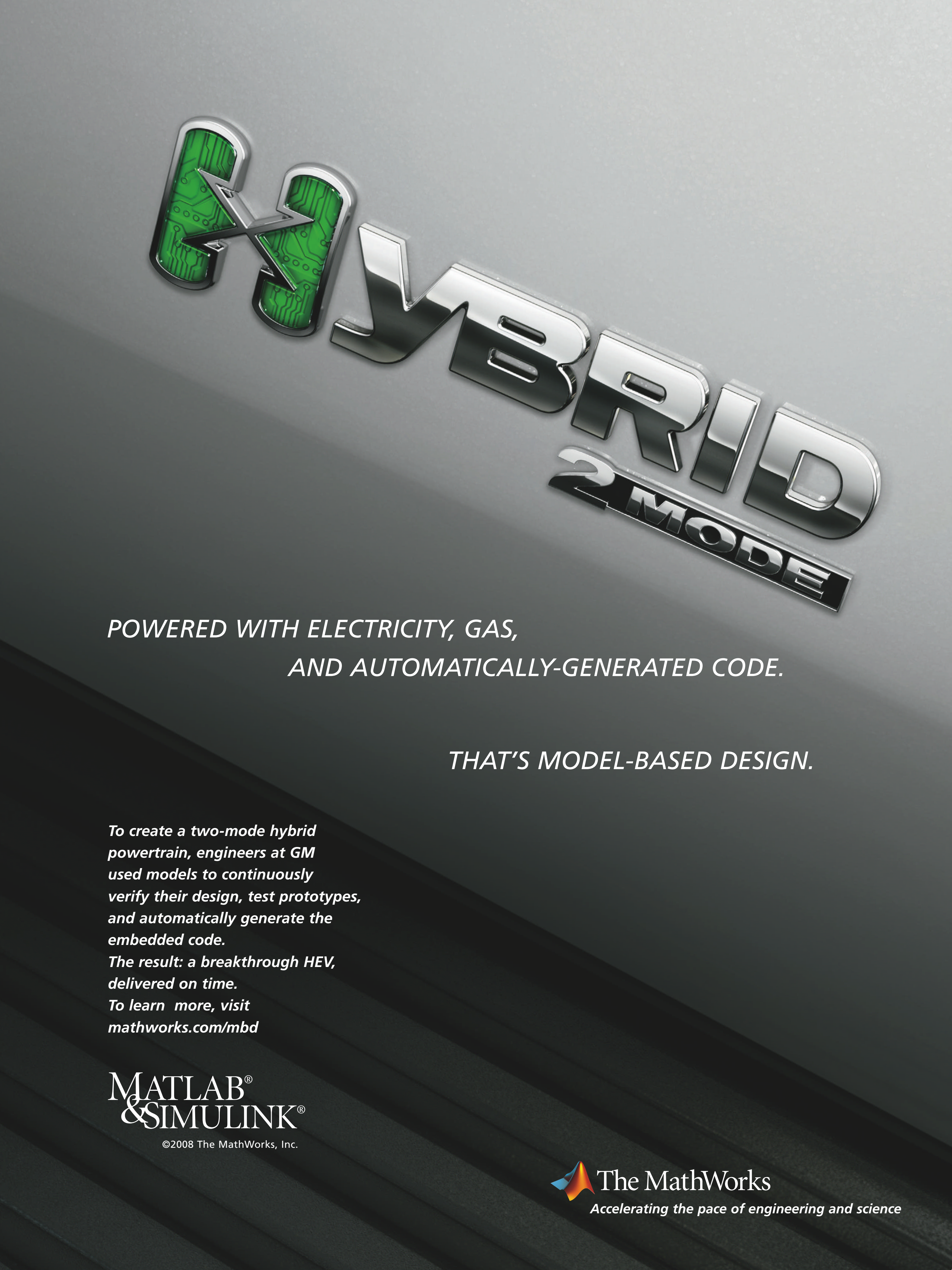
Neurostimulators improve quality of life

Chronic-pain sufferers can benefit from the Eon Mini neurostimulator from the St Jude Medical Neuromodulation Division. The device is a rechargeable spinal-cord stimulator that treats chronic pain of the torso and limbs. The device gained US Food and Drug Administration and European CE (Conformité Européenne) mark approvals in April 2008 and received Australian Therapeutic Goods Administration approval in February 2009. An article in the April 1, 2009, issue of *Test & Measurement World* recounts the efforts of Eddie Abshire, senior test engineer at St Jude Medical Neuromodulation Division, in assisting in bringing the device to market. As a result of his work, *Test & Measurement World* readers voted him Test Engineer of the Year. "It's … important to make sure that these systems are safe and that the patients enjoy a good quality of life," says Abshire.



Percutaneous leads—those that physicians can insert using a needle—deliver current pulses from the Eon Mini neurostimulator to appropriate points along the spinal cord, where the pulses interrupt pain signals as they travel to the brain. As an alternative to using the percutaneous leads, neurosurgeons can surgically implant paddle leads to provide improved directivity (images courtesy St Jude Medical).

Doctors typically implant the 18-cc Eon Mini neurostimulator above a patient's buttock area; the device is small, and its maximum implant depth is 2.5 cm, so it is less obtrusive and more comfortable than larger devices. The device generates 0- to 25.5-mA current pulses having widths from 50 to 500 µsec at frequencies of 2 to 1200 Hz. A physician determines the optimum current-pulse program; a portable controller lets the patient adjust the program to accommodate changing pain profiles throughout the day. A 16-contact header connects with St Jude Medical's line of percutaneous and paddle leads.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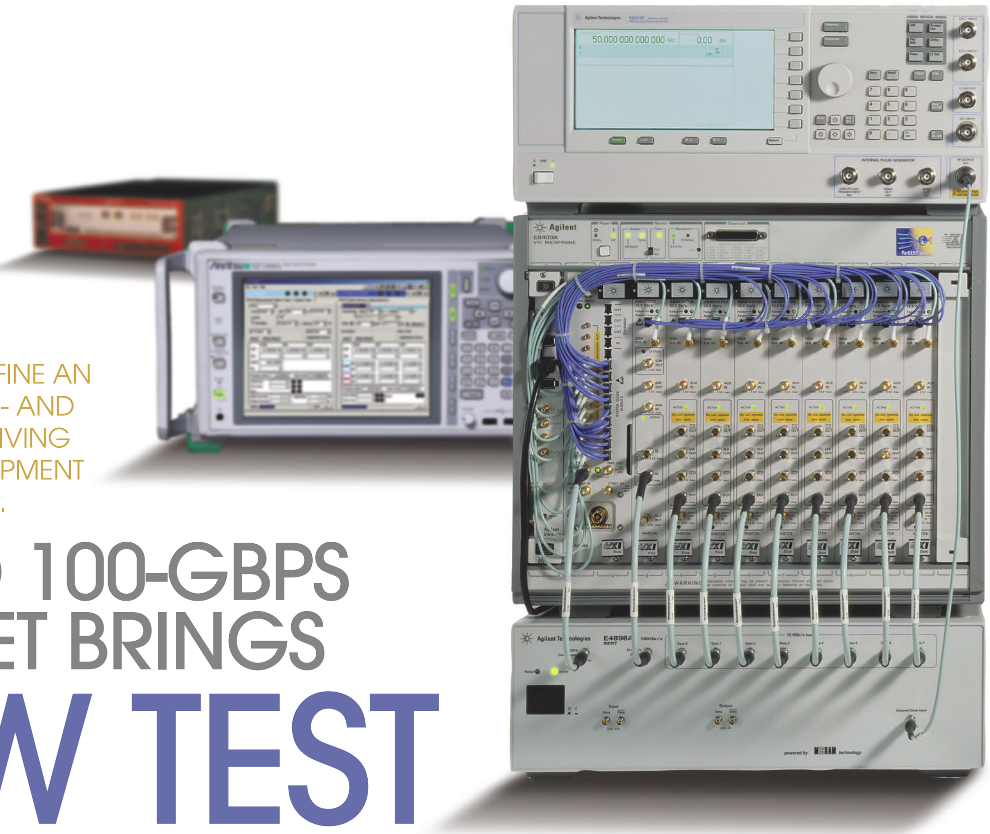

IEEE P802.3BA WILL DEFINE AN ARCHITECTURE FOR 40- AND 100-GBPS ETHERNET, GIVING RISE TO NEW TEST EQUIPMENT AND TEST TECHNIQUES.

40- AND 100-GBPS ETHERNET BRINGS NEW TEST CHALLENGES

BY MARTIN ROWE • SENIOR TECHNICAL EDITOR, *TEST & MEASUREMENT WORLD*

Internet and data-center users always demand higher bandwidth to carry voice, data, and especially video. Because of that demand, today's 10-Gbps optical and electrical links are running out of capacity. Data centers and core networks need faster links, according to participants at the OFCNFOEC (Optical Fiber Communication Conference and Exposition/National Fiber Optic Engineers Conference) in March 2008 (**Reference 1**). At the time, the IEEE P802.3ba Ethernet task force was developing a standard that will define an architecture for 40- and 100-Gbps Ethernet (**Reference 2**). Although IEEE P802.3ba is still in the works, engineers worldwide are beginning to develop products that employ these links, and those products will need testing. Much of the testing for IEEE P802.3ba will use 10-Gbps technology, but some tests will require new equipment and new techniques.

FLEXIBLE ARCHITECTURE

John D'Ambrosia, senior scientist at Force10 Networks and chairman of the IEEE P802.3ba task force, leads a team of engineers that is working out the details of IEEE P802.3ba. Although details are still forthcoming, the IEEE P802.3ba task force has defined a general architecture, the architecture's protocol sublayers, and how those sublayers function (**Reference 3**). **Figure 1** shows a simplified diagram of the architectures for 40- and 100-Gbps optical networks. Although the architectures differ slightly, IC manufacturers could implement both in the same part.

For optical networks, IEEE P802.3ba defines the PCS (physical-coding sublayer), the PMA (physical-medium-attachment) sublayer, and the PMD (physical-medium-dependent) sublayer. Both 40- and 100-Gbps implementations can use 10-Gbps fiber PHY (physical) links. In the future, the same architecture will support 100-Gbps links using four 25-Gbps lanes. IEEE P802.3ba also defines two additional sublayers for copper connections.

The PCS performs 64b/66b encoding on an aggregate 40- or 100-Gbps data stream to produce 66-byte blocks. It then sends the blocks across four lanes for 40-Gbps transmission or 20 lanes for 100-Gbps transmission. "We chose 20 lanes because [20] is divisible by one, two, four, five, and 10," says D'Ambrosia. So far, it appears that PCS will operate with four or 10 lanes. Each of the 20 PCS lanes will include a lane marker that identifies a lane and provides timing information for each data block (**Reference 4**). **Figure 2** shows how the 66-bit blocks will travel within the PCS lanes. Distribution of the blocks occurs in a round-robin fashion across the PCS lanes. A striping process divides the blocks across the PCS lanes.

The PMA sublayer matches the number of PCS lanes to the number of lanes that a physical layer requires. For 40-Gbps transmission, the PMA sublayer maintains four lanes. For 100-Gbps transmission, the PMA sublayer converts 20 XLAUI (40-Gbps-attachment-unit-interface) or CAUI (100-Gbps-attachment-unit-interface) lanes to 10 XLAUI or CAUI lanes. The PMD sublayer provides the final interface to a physical medium. **Table 1** describes these physical media and their respective transmission distances. In general, 40-Gbps links will find use in data centers, and 100-Gbps links will operate in core networks.

IEEE P802.3ba's flexible architecture supports long-reach and extended-reach optical links, which use WDM (wavelength-division multiplexing) across SMF (single-mode fiber). Short-reach links use multiple fibers, each carrying a different lane. Because optical and electrical components that send and receive 10-Gbps signals are now available, initial implementations of 40- and 100-Gbps transmission systems will use four and 10 10-Gbps lanes, respectively. Four-lane implementations using 25-Gbps links—actually, 25.78125 Gbps due to encoding—will take some time to appear, but communications carriers plan to use WDM, which has four wavelengths, on single-mode fiber for 40-km transmissions (**Reference 5**).

TESTING P802.3BA

Because 10-Gbps lanes will appear first, you'll be able to use your 10-Gbps optical test equipment to measure parameters such as timing jitter, amplitude, and BER (bit-error rate). You can test only one transmission path at a time, however, until equipment that can test

AT A GLANCE

- Today's 10-Gbps optical and electrical links are running out of capacity.
- The IEEE P802.3ba standard defines the PCS (physical-coding sublayer), the PMA (physical-medium-attachment) sublayer, and the PMD (physical-medium-dependent) sublayer.
- Initial implementations of 40- and 100-Gbps transmission systems will use four and 10 10-Gbps lanes, respectively.
- When testing an implementation that uses four or 10 fibers or wires in each direction, you must individually test each path.
- You'll be able to use your 10-Gbps optical test equipment to measure parameters such as timing jitter, amplitude, and BER (bit-error rate).

TEST EQUIPMENT FOR 40- AND 100-GBPS ETHERNET

Because testing the 10-Gbps physical lanes that comprise 40 and 100 links is similar to testing 10-GbE (gigabit Ethernet), you can test the physical layer of 40 and 100 GbE with oscilloscopes, BER (bit-error-rate) testers, and optical spectrum analyzers. Currently, little test equipment is available for testing at 100 Gbps, but some is starting to reach the market. For example, Ixia used its 100GE development-accelerator system to perform a proof-of-concept demonstration of 100-Gbps Ethernet in June 2008 at NXTcomm08 (Figure A and Reference A). The system, which Ixia formally announced to the public in September 2008 and began shipping in February 2009, generates and analyzes Layer 2 Ethernet traffic at 100 Gbps.

Among other recently introduced test equipment for Ethernet are products from Agilent, Anritsu, and Centellax. For example, Agilent Technologies' E4899A serial-BER tester for research labs and standards bodies lets you perform BER tests at 40 and 100 Gbps (Figure B and Reference B). In March, Agilent introduced the N4931A optical-modulation analyzer, which analyzes 40- and 100-Gbps optical signals using microwave techniques. Anritsu recently announced I/O cards for its MP1800A signal analyzer, which lets you modulate and analyze 40- and 100-Gbps optical signals (Figure C and Reference C). Further, Centellax recently introduced a 40-Gbps clock and data multiplexer. You can use the instrument to perform BER measurements on physical-layer links. In addition, PicoSolve, which Exfo acquired in February, manufactures PC-based optical sampling oscilloscopes that can characterize and monitor high-speed transmissions at 40 Gbps.

Although 10-GbE test equipment will get things started, IEEE P802.3ba will likely give rise to new test equipment. For example, testing with a four- or 10-lane BER system takes less time than using a single-channel instrument. Protocol analyzers that decode the data blocks into Ethernet packets will also help. In addition, testers that inject unexpected alignment blocks and remove expected alignment blocks will help

Figure A Ixia used its 100GE development-accelerator system in a demonstration of 100-Gbps Ethernet.

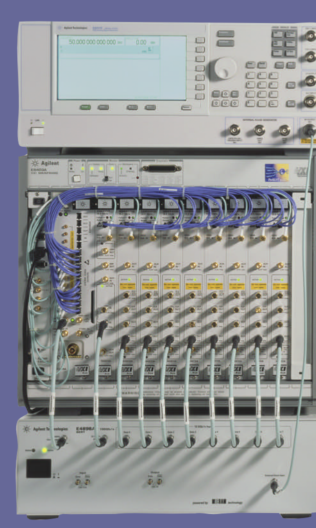

Figure B Agilent Technologies' 40/100-Gbps BER tester lets you test physical layers for bit errors.

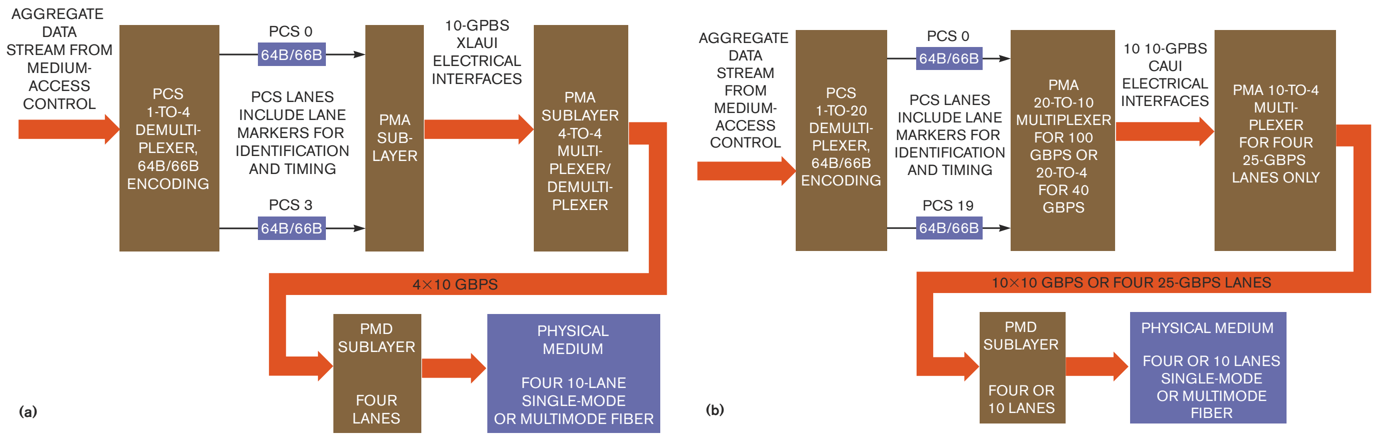

Figure 1 The IEEE P802.3ba architecture defines three sublayers (brown boxes) for optical transmission that support four data lanes to achieve 40 Gbps (a) or four to 10 data lanes to achieve 100 Gbps (b).

four or 10 lanes becomes available. "Tests for the individual optical lanes will be very similar to tests for existing 10-Gbps technology," says Edward Nakamoto, director of hardware for Spirent Communications. Testing multilane Ethernet will require you to start by individually testing each lane for signal integrity and BER (see **sidebar** "Test equipment for 40- and 100-Gbps Ethernet"). When testing four or 10 10-Gbps lanes, you must illuminate all lanes, preferably with data, and perform BER measurements on each lane. You then must modulate the laser with the data. **Reference 4** also describes modulation techniques that are in development for use with single-mode fibers for long-haul transmissions.

you test your network link. IC manufacturers are currently working with test-equipment makers to develop the components that will carry the protocol sublayers. One example is Altera, which has announced that its high-end FPGAs are available with 24 transceivers that can communicate at 11.3 Gbps. Thus, one device can handle 10 or 11 10-Gbps lanes with additional transceivers available for generating errors and monitoring traffic. The FPGA can connect directly to optical modules, and it can hold the PCS (physical-coding sublayer) and PMA (physical-medium-attachment) sublayer in the device. If designers use the Altera device, however, test engineers won't have access to the interface between the PCS and PMA sublayers for testing. It's an engineering trade-off that you may have to make.

The IEEE P802.3ba task force also plans to define an architecture that provides for implementations that use four 25-Gbps physical lanes to achieve 100-Gbps throughput. These implementations will need new technology in the form of ICs and optical components that will run at those speeds. Modulation methods such as DP-QPSK (dual-polarization quadrature-phase-shift keying) and DQPSK (dual quadrature-phase-shift keying) that can handle those speeds are under development. The PSK (phase-shift-keying) methods could solve problems due to polarization-mode and chromatic dispersion (Reference D).

The higher data rate will require engineers to develop electrical and optical components that can reach that speed, and test equipment will need to keep up. For example, real-time oscilloscopes will need even more bandwidth than the current 30-GHz, state-of-the-art technology available in LeCroy's WaveMaster 8 Zi series (Reference E). You also need BER testers, clock-recovery units, optical spectrum analyzers, and other equipment that can work with signals at those speeds. Stressed-eye testers will also let you test optical receivers for the added signal distortion that will occur at the higher bit rate.

Figure C I/O cards for Anritsu's MP1800A signal analyzer let you modulate and analyze 40- and 100-Gbps optical signals.

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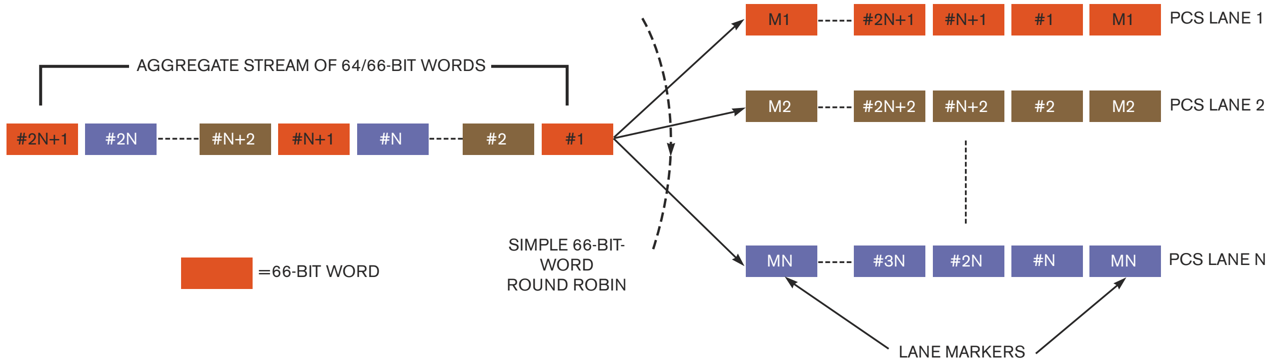

Figure 2 The PCS places 66-bit blocks into 20 lanes that include lane markers (courtesy Ethernet Alliance).

Michael Fleischer-Reumann, strategic-product planner at Agilent Technologies, notes that you can test an optical medium by generating PRBS (pseudo-random-bit-sequence) test patterns with a BER tester. When testing an implementation that uses four or 10 fibers or wires in each direction, you must individually test each path. "When testing a WDM-multimode fiber with four or 10 wavelengths, you'll need a tunable laser," he says. Testing individual lanes is a good start, but you must also test lane timing and skew. When you are using WDM fiber, each data stream uses a unique wavelength, but each wavelength has a different propagation speed. Optical receivers must compensate for timing differences in transmissions.

To achieve that compensation, IEEE P802.3ba will define alignment blocks at the PCS that convey timing information. Alignment blocks appear once every 16,384 blocks in a data stream (**Reference 5**). Receivers use those blocks to realign the lane blocks before reconstructing the data stream. "The standard is very insensitive to skew," says Jeff Lapak, 10 Gigabit Ethernet Consortium manager at the UNH-IOL (University of New Hampshire Interoperability Lab). "It will be difficult to break alignment as part of our testing, but we'll do it." Lapak intends to test for skew-induced errors by removing alignment blocks from where they belong and inserting them where they don't belong in a data stream. Unfortunately, detecting errors is complicated because testers may not have access to each sublayer. IC designers will try to integrate the sublayers into as few devices as possible, so it's likely that the PCS, PMA sublayer, and PMD sublayer won't reside in three ICs. At least two—and perhaps all three—may reside in a single IC.

Lapak is waiting to see how IC designers package the sublayers before UNH-IOL engineers and students develop test tools. "IOL wants to test where sublayer interfaces will be the most consistent among manufacturers," he says. Companies such as Sarance Technologies have begun implementing 40- and 100-Gbps Ethernet cores into Xilinx FPGAs (**Reference 6**). This implementation combines the PCS and the PMA sublayer, and it adds MAC (media-access control), a layer above PCS. Because the sublayers reside in ICs, the interfaces between the devices will be electrical regardless of the physical-transport medium. Electrical crosstalk will be a significant challenge. "Interference and crosstalk may occur on the electrical side," says Toshihiro Suzuki, assistant manager at the product-planning center of the marketing division of Anritsu and a member of the IEEE P802.3ba task force. "At the design and verification stage, engineers must test for crosstalk and interference by using a multichannel pattern generator," he says. You'll then need an oscilloscope to look at adjacent lanes—if you can get access to them.

At the system level, you must test the multiplexing and demultiplexing functions. "Tests [must] be developed [for] the breaking up of the traffic into multiple lanes," says Spirent's Nakamoto.

Lapak of the UNH-IOL goes a step further, saying that he expects to test block encoding and decoding by reversing the order of the data on PCS lanes. "You don't know which lane will carry a block," he says. "Every lane has to be able to carry blocks from any other lane." Thus, he expects to develop test tools to reverse the order of the lanes and test whether a receiver will receive alignment information and reconstruct the data.**EDN**

TABLE 1 TRANSMISSION DISTANCES FOR PHYSICAL MEDIA

Minimum distance	Medium	40-Gbps Ethernet	100-Gbps Ethernet
1m	Backplane	40GBaseKR4	
10m	Copper cable	40GBaseCR4	100GBaseCR10
100m	OM3 multimode fiber	40GBaseSR4	100GBaseSR10
10 km	Single-mode fiber	40GBaseLR4	100GBaseLR4
40 km	Single-mode fiber		100GBaseER4

A version of this article appears on the *Test & Measurement World* Web site, www.tmworld.com/article/CA6640178. There you will find a list of test equipment introduced at OFCNFOEC 2009.

For a list of references cited in this article, as well as more information on the companies it mentions, go to www.edn.com/090423df.

POWER fortunes

ESTIMATING POWER IN FPGA DESIGNS

AS FPGAs ENTER NEW APPLICATIONS, DESIGNERS MUST ESTIMATE POWER CONSUMPTION EARLY, CLOSELY WATCH IT, AND THEN ATTEMPT TO MEASURE THE RESULTS.

BY RON WILSON • EXECUTIVE EDITOR

In simpler times, FPGA power consumption was a simpler issue. In the traditional applications of high-capacity FPGAs, such as expensive network routers, telecommunications switching gear, and prototype boards for ASIC designs, all you needed to know was how much peak power the FPGA could consume and how to provide cooling for its operating appetites. Today, the world is different. "Previously, FPGAs were not a serious alternative for production," says Rahul Shah, director of customer solutions at design-services vendor eInfochips. "But with shorter life spans for products and more emphasis on time to market, we are seeing customers want to go into production with FPGAs. So, more focus is now going onto the power consumed in the FPGA."

Facing tight enclosures with minimal cooling, tight budgets, and sometimes even battery power, designers must be able to get accurate power estimates on their FPGA designs early in the design cycle. They must be able to refine those estimates throughout the cycle so that they can apply aggressive power-management techniques (**Figure 1**). And they must be able to accurately measure the power of the resulting design. As it turns out, none of these requirements is trivial.

EARLY ESTIMATION

Ideally, design teams could begin to explore the power-consumption implications of their designs from the beginning, when they are formulating the design requirements and exploring algorithms. No widely used tools are available, however, for estimating power consumption from a set of design requirements or even from an algorithm. So, when the members of a design team have the most leverage over power consumption, they are flying nearly blind. Only experience with similar applications is there to guide them. "Our engagement with power issues begins at the specification stage," says Raj Kothandaraman, lead FPGA designer at Wipro Technologies. The company built up an internal design method with an emphasis on power management. Through that method, design teams accumulate data—vital to early power estimates—on switching activity for various kinds of structures. Such history can give the design team some qualitative idea of the implications of the design requirements and even the power costs of algorithm decisions.


FPGA ANALYSIS
PROPHECIES

Shah describes a similar dependence on experience. "You define the power budget early, considering things you can know early, such as voltage levels, input-data characteristics, and the major functional blocks in the proposed system," he says. "Often, we will look at static power first since it is less sensitive to detailed information that we won't have early in the design. Then, as we understand more about the design, we will begin estimating dynamic power, and, finally, we will begin to estimate the impact of power-saving strategies. There are no formal tools for this estimation process. So we have to rely on data-sheet information, spreadsheets, and our own experience with FPGAs."

These early estimates are necessarily vague because much of the information necessary for an accurate estimate—detailed toggle-rate information, actual data flows, routing loads, and power-management features, for instance—doesn't yet exist. But it is still necessary to have a conservative estimate of the final system. Mike Morgan, principal design engineer at design shop North Pole Engineering, points out that the customer's decision to use an FPGA in the first place often results from a tight design schedule. That same pressure demands that the board design start concurrently with the FPGA design. And the board design, early on, needs estimated power. "In general, when I start a PCB [printed-circuit-board] design centered around a Xilinx device, I conservatively estimate power consumption and design or specify power supplies, distribution, and heat dissipation based on this [estimation]," he says.

AT A GLANCE

- FPGAs are entering power-critical applications.
- Tools for early power estimation are surprisingly accurate.
- Power-analysis tools add a lot, but they depend on your knowledge of the application.
- Measuring FPGA power can be devilishly difficult.

REFINING THE ESTIMATES

As the design progresses from algorithms through definition of blocks and on to the beginnings of implementation, the design team gets more specific data about signals, toggle rates, and the structure of the blocks. At this point, still long before freezing the RTL (register-transfer-level) logic, design teams begin to use vendor-supplied power-estimation tools to improve the accuracy of their power estimates. "Tools from the FPGA vendor—typically, Excel spreadsheets—become important," Kothandaraman says. These tools can absorb huge amounts of information about the design. For example, Ian Milton, a member of the technical staff at Altera, says that the company's Early Power Estimator allows designers to enter activity levels on registers, clock frequencies, enable-pin duty cycles, block-RAM configurations, read/write duty cycles, statistical characteristics of input signals, estimates of the number of logic elements in a block, and so on.

For the most part, vendors have designed these spreadsheets so that design teams can enter architectural information early, leave many of the inputs at default settings, and get a crude estimate of power. As the team learns more about the design, they can replace more of the defaults with design data, refining the power estimate. "We try to encourage people to use the default settings early on," Milton says. The reason for relying on the defaults is that the vendors have built what amount to intelligent systems into those default settings, deriving defaults from actual measurements of large numbers of designs. For example, Altera's tool estimates how many of the nets in a design will have critical timing and how many will have timing slack and, employing that estimate, determines how many logic cells will be in high-performance mode and how many will be in low-leakage mode.

Even with the defaults, though, the design team still has to understand a great deal about the behavior—rather than the implementation—of the design to get the best estimate. "We look at input-data patterns," says eInfochips' Shah. "From there, we look at clock-tree power. Then, we ask whether the inputs are going into a datapath or a control path and try to understand what that [placement] implies about the activity levels inside. There are no predefined calculations that will tell you these things. You have to rely on experience and methodology. You try to institutionalize the knowledge you gain from each new design by creating templates and processes. Unfortunately, the vendors have not defined a clear methodology for doing a power-aware design, so every design team around the world is doing this job in its own way."

Wipro's Kothandaraman agrees that one of the most powerful weapons for using the early-estimate spreadsheets is experience. "For instance, we have estimates for I/O activity based on previous designs in the same application area," he says. "That [information] is a great help in estimating the final power."

The accuracy of these early estimates

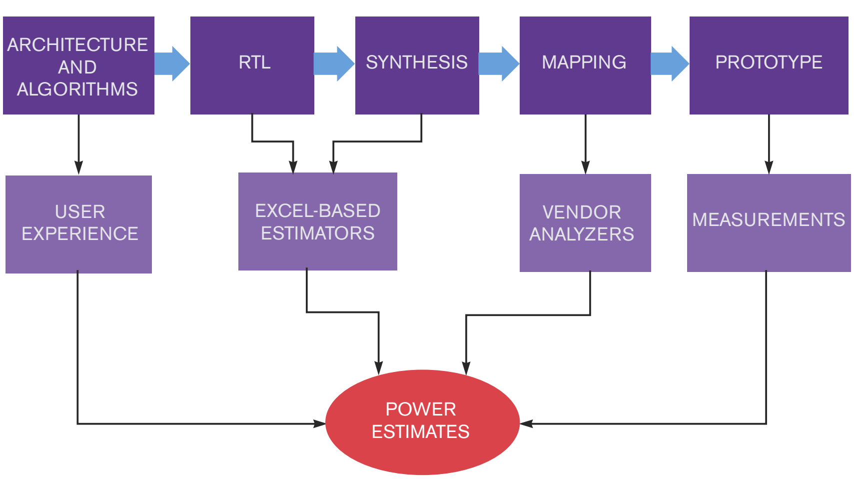

Figure 1 Through the design flow, designers refine their estimates of FPGA power consumption.

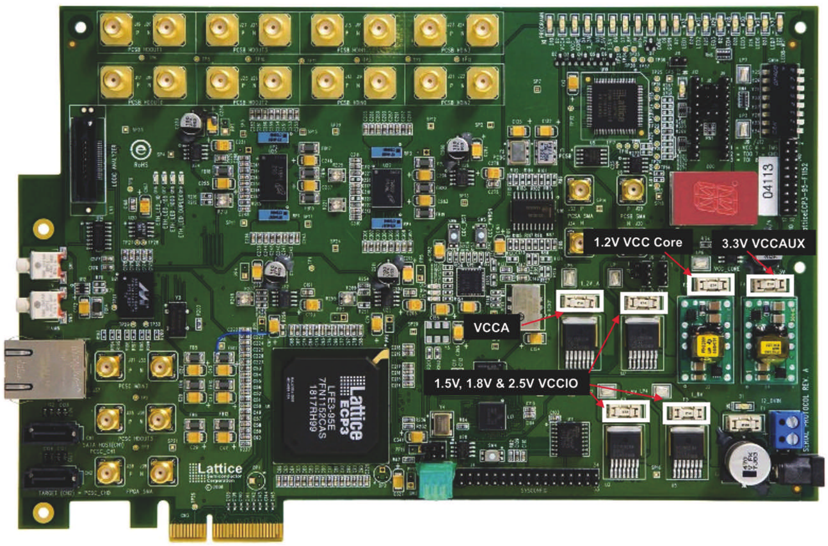

Figure 2 Development boards, like this one from Lattice Semiconductor, often provide low-impedance access points for monitoring current on the FPGA's supply rails.

is an interesting issue. "These tools have really improved recently," Kothandaraman says. "Years ago, there were lots of correlation problems with the tool results. But today, you can expect your early estimates to be within 20 or 30% of the final power consumption."

Shah agrees. "Vendors are becoming more sensitive to power issues," he says. "They are providing more accurate models and more Webinars on how to use the tools; this estimation process was not so accurate before."

But Kothandaraman warns that the design process has a way of undermining its own power estimates. "As we go along, we tend to add more logic to the design," he says. "That [tendency] kills our early power estimates."

As the tools improve, the problems are getting more complex. A modern FPGA has multiple power rails, including core, auxiliary, I/O, and analog rails. All these rails are important in the analysis of parts, according to Jatinder Singh, an application engineer at Lattice Semiconductor. Each of these rails may be operating at a different voltage, and there may be two or more I/O voltages. Some devices may have separate core-power rails that you can shut down independently, and each of these power rails may respond to a different measure of activity. So the early-estimate spreadsheets must be explicit about separating activity in the logic fabric from I/O activity, monitoring SERDES (serializer/deserializer) activity as a separate issue, and so on. Further, the growing plethora of embedded functions in modern FPGAs adds complications. Estimates must encompass the configuration of and activity on DSP blocks and block RAMs, for instance.

FINAL ESTIMATES

As the design team creates RTL logic, the inputs to the spreadsheet estimators can become more precise. Once there is enough logic to perform simulation, however, a new category of vendor tool becomes available: the power analyzer.

These tools work in a fundamentally different way from spreadsheet estimators. "Once you have good RTL, you can synthesize and map the design," says Altera's Milton. "Then, you can run a simulation and extract a value-change dump. This [step] will provide actual toggle rates on every node in a block." A power analyzer reads this data, combines it with the mapping files that indicate the actual LUT (look-up-table) and routing-segment configuration at each node, and produces power calculations that, in principle, are as accurate as the vendor's device models. "The tools know things the customer couldn't know, such as the actual wire segments the mapping tool used to connect two logic elements," Milton says. "And the tools understand the differences between FPGAs and ASICs. For example, in an ASIC, if you have an AND gate with one input low, there is no significant activity in the gate; the output is low. But, in an FPGA, the output buffer will stay low, but there is significant power-consuming activity within the LUT. Every change in the active input is causing, in effect, a read cycle in a little RAM."

Power analyzers should be the last word in estimating the power consumption of an FPGA design. Accuracy is a two-edged sword, however. If you put in the wrong input data, you get precisely wrong results. One problem is trying to employ too precise a tool too early, according to eInfochips' Shah. "Don't update your power estimates with incomplete RTL," he says. "That remaining few [percentage points] of the RTL may turn out to consume 30% of the power."

Also, Shah warns that seemingly small changes to the RTL can make big changes in power consumption. "FPGA mapping is not as deterministic as ASIC layout," he says. "Routing depends on the remaining resources in the device. If you are filling up the FPGA, you may find that LUTs that are connected to each other are nowhere near adjacent to each other." Increased distance would increase power dissipation for each toggle of signals passing between the LUTs.

Wipro's Kothandaraman also counsels caution. "The power-analyzer tools do not always improve our understanding of the power consumption of our design," he says. "Partly, this [drawback] is because we keep adding logic until late in the design. Also, the tools don't always do the most powerful job of processing the simulation dumps. And the value of the predictions depends on the value of the simulation scenarios you choose to run. But there are many operating modes in a modern FPGA design.

POWER ANALYZERS SHOULD BE THE LAST WORD IN ESTIMATING THE POWER CONSUMPTION OF AN FPGA DESIGN.

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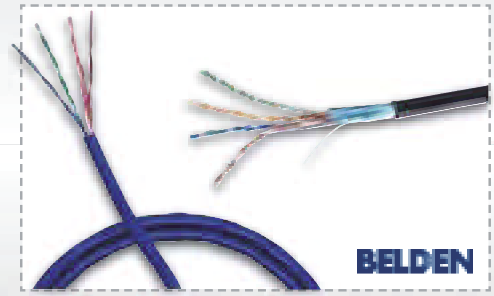

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308-0090	Jam Nut Receptacle, RJ11 to RJ11	81.71
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- Max. recommended pulling tension: 40 lbs.
- Min. bend radius (install)/minor axis: 1 inch

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216-0445	Industrial Ethernet Cable (CX/1000)	366.53

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Features

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Stock No.	Description	Price
886-0385	IEC Contactor, 9 Amp, 110V/120V	26.22
886-0421	IEC Contactor, 12 Amp, 110V/120V	27.96
886-0424	IEC Contactor, 25 Amp, 110V/120V	45.87
886-0426	IEC Contactor, 32 Amp, 24V	62.48
886-0431	IEC Contactor, 40 Amp, 110V	98.29

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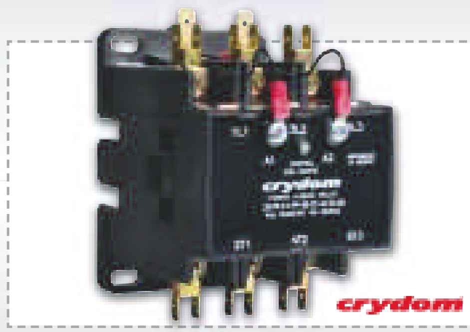

RHP Series Hybrid Contactors

Crydom has combined solid state and mechanical switching technologies to create the RHP Series. Crydom's Hybrid SSR technology utilizes contactless solid state turn on and turn off performance, coupled with the very low on state power dissipation characteristic of contactors.

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- No heat sinking required

Stock No.	Description	Price
682-0494	40A/600VAC, 20-26VAC Input	125.00
682-0495	40A/600VAC, 100-130VAC Input	125.83
682-0496	40A/600VAC, 208-240VAC Input	126.25
682-0506	40A/240VAC, 4.5-5.5VDC Input	128.33
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Stock No.	Description	Price
909-0645	RAD-ISM-900-EN-BD	1,734.00

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Motor Overload Relay (Protection Relay)

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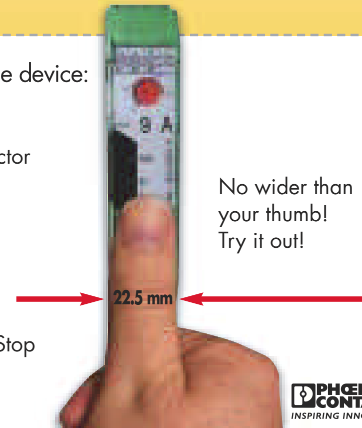

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- System availability is maximized by the nearly wear-free switching ability of the contactors

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909-0648	24 VDC Input, 2A Output Current	139.83
909-0649	230 VAC Input, 2A Output Current	147.90
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908-0212	J86-4400 Keyboard	476.53

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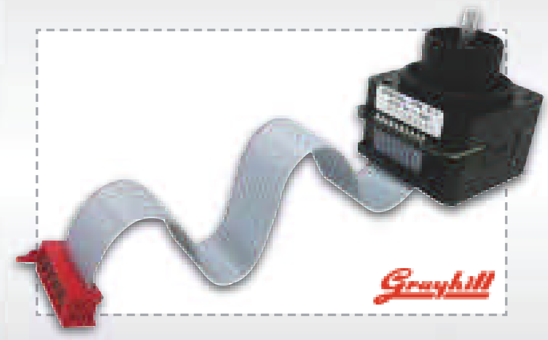

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381-1338	20 AWG (PK/500)	33.68	381-1342	14 AWG (PK/500)	39.61

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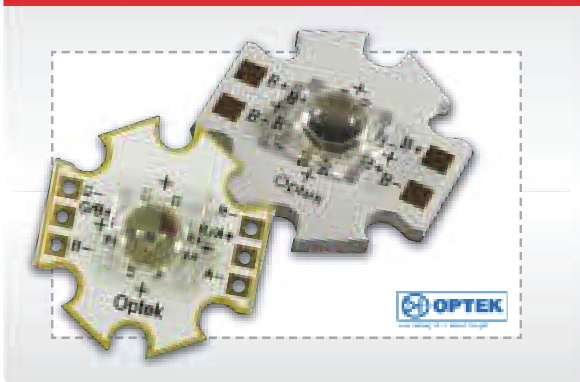

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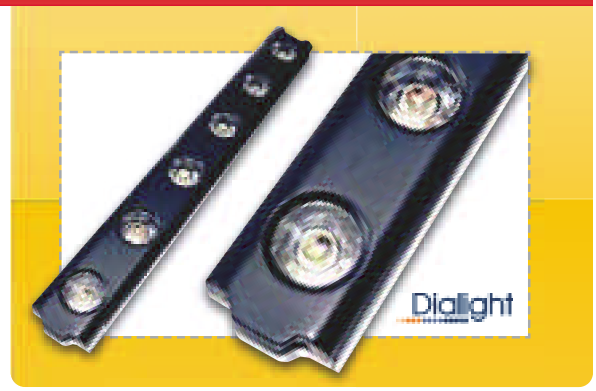

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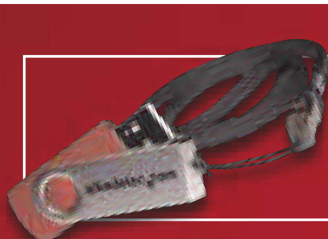

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ANOTHER INCREASINGLY IMPORTANT VARIABLE COMES FROM THE FACT THAT MANY SYSTEM-IN-FPGA DESIGNS NOW INCLUDE MICROPROCESSOR CORES.

It is a big challenge to generate vectors that will actually stimulate worst-case toggle rates." On this last point, Kothandaraman says that Wipro is trying to establish a feedback loop within its design teams to capture experience in creating vectors for power estimation. But that work is still in progress.

The company knows from experience what worst-case traffic patterns should be for memory activity in networking equipment, for instance. In applications such as media processors or set-top boxes, however, identifying a worst-case video clip may take a major simulation effort all by itself. Kothandaraman adds that it is important to study not just logic-fabric activity, but also what's going on in the other parts of the FPGA. In both media and networking applications, memory blocks and SERDES may be more important to the power consumption than the logic fabric itself.

Another increasingly important variable comes from the fact that many system-in-FPGA designs now include microprocessor cores. This fact makes the power scenarios depend not only on the RTL logic, the mapping, and the vectors, but also on the firmware. Just as the hardware design team is freezing RTL logic and trying to pin down power data, the software team may be just getting working silicon and entering their period of highest rate of change for the firmware, with huge implications for power. The bottom line, according to Kothandaraman, is that you must make careful use of power-analysis tools. He warns that the early-estimation tools may end up giving you more accurate results than the analysis tools do.

MEASURING THE RESULTS

One big advantage of FPGAs is that, in the case of any uncertainly, you can always program up a part, drop it into a prototyping board, and see what it does. In the case of FPGA-power measurement, however, this problem is far from trivial. In part, measuring FPGA power is complicated because there are so many power rails and pins. In practice, the multiplicity of pins per rail means

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you have to measure voltage and current closer to the regulator, rather than closer to the chip, risking errors on high-current transients. It helps that most FPGA vendors provide access for current probes on their evaluation boards (**Figure 2**).

A more serious problem is that FPGA power-rail current tends to be dynamic. "As you move to finer geometries, the inrush current when you first apply power to an FPGA is often greater than the steady-state current," says Lattice's Singh. "You must characterize SRAM-based FPGAs in three sections—inrush, initialization, and programming—in addition to steady-state current."

Kothandaraman describes another problem. "On some devices, there is also a current pulse between the programming and operating modes," he says.

North Pole's Morgan reports similar experience. "Once we have a prototype, power demands are one of many items we verify as part of the design-verification process," he says. "We are most concerned with identifying the peak current demand [and] peak inrush and reporting the observed peak and average operating quiescent currents to ensure that our power supplies and dc/dc converters are operating optimally, traces and power vias are appropriately sized, junction temperatures do not exceed data-sheet specifications, and so on." As Morgan points out, the dynamics on the power pins create their own measurement problems. Sudden bursts of activity in a highly parallel structure within the core or sudden bursts of memory traffic may produce narrow current spikes. These spikes may not contribute much to rms (root/mean/square) power, but they can fry metal on advanced-geometry FPGAs. The spikes also cause IR drops, which the decoupling-capacitor network needs to handle.

The problem is not getting any simpler. Vendors are making available more sophisticated power-management techniques, including clock gating, reduced-voltage operation, and some degree of power gating. According to one source, National Semiconductor is working with some FPGA designs to apply dynamic voltage-frequency scaling to the core-logic fabric of an FPGA, claiming that it is possible to achieve a 30 to 40% reduction in power in this way. Each of these techniques makes the problem of estimating—and measuring—power that much harder. Shah says that eInfochips often manipulates the configuration of FPGAs in the prototype, attempting to isolate a functional block and get an accurate power measurement on it. "This is an interesting problem," he says. "Measuring power is a bit challenging on the board."

Estimating and measuring FPGA power is a difficult problem. Design teams need early worst-case estimates and accurate data throughout the design to make decisions on power-management strategies. When they are done, they also need to know what they've accomplished. We can expect vendor tools to improve, but it may be deep experience in an application and with an FPGA architecture that ends up making the most difference. EDN

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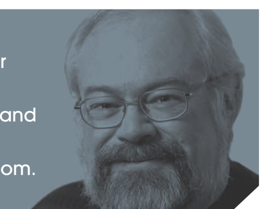
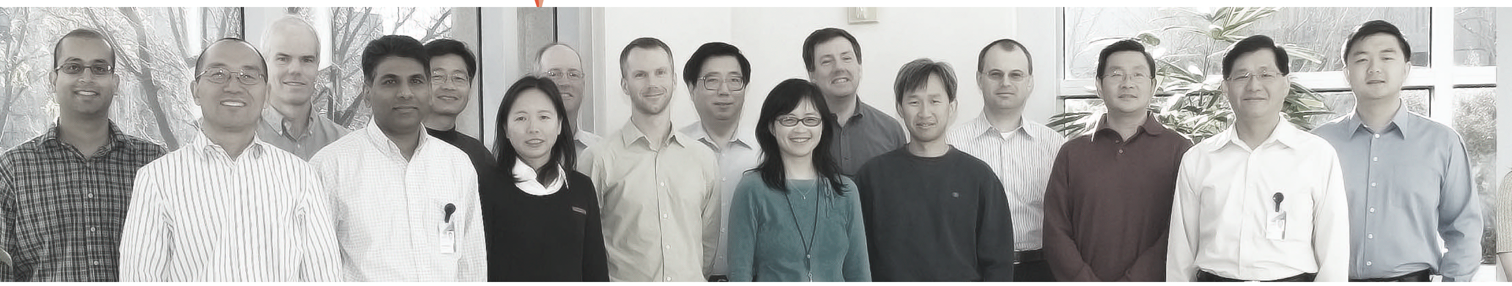
You can reach Executive Editor Ron Wilson at 1-510-744-1263 and ronald.wilson@reedbusiness.com.



EDN's 2008 INNOVATOR AND INNOVATIONS OF THE YEAR:

AND THE WINNER IS . . .



For more details on the winners and all of the finalists, as well as photos from the festivities, visit www.edn.com/innovation.

A challenging economic environment in 2008 brought out the best in several members of the electronics industry. And *EDN*'s annual Innovation Awards program has once again honored the most innovative technological advances as well as the designers behind those advances. This year, the judges—a team effort that involved *EDN*'s editorial staff and you, the readers of *EDN* and edn.com—faced a serious challenge to decide among closely matched and highly qualified entrants in 26 product and technology categories. In addition, we considered nominations for 2008's Best Contributed Article and Innovator of the Year.

Read on to learn who took home top honors at this year's awards ceremony, which took place March 30 in San Jose, CA.

INNOVATOR OF THE YEAR

THE STRATIX IV 40-NM-FPGA-DESIGN TEAM AT ALTERA

Approaching the design and development of Stratix IV, Altera's 40-nm-design team's goal was to optimize time to market, performance, manufacturability, and cost. With time-to-market pressures and complex design issues, Altera had the challenge of closing all gaps under a schedule that was much shorter than the regular development cycle. The team formed 12 joint development teams with TSMC (Taiwan Semiconductor Manufacturing Co) to address issues such as power/performance balance, modeling, test-chip planning, DP-SRAM (dual-port SRAM), polyfuse, DFM (design for manufacturability), standard cells, RF/analog, ESD (electrostatic discharge), and ELK (extreme low k). The development of these "tiger" teams and their close collaboration helped to shave months off the manufacturing and IC-design process.

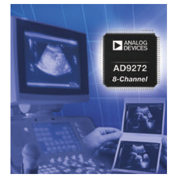
Another core area the 40-nm-design team addressed was power management. The team used five innovative methods to reduce leakage current: increased transistor threshold voltage using doping, increased transistor channel length, the application of thicker gate oxide, increased transistor threshold voltage using programmable-power technology, and decreased supply voltage. As a result, it was able to deliver 50% lower power and 35% higher performance than competing FPGA devices. The team also built upon Altera's proven transceiver technology to increase the transceiver's performance to 8.5 Gbps, providing even better signal integrity and broadening its range of protocol support.

One of the most valuable strategies the 40-nm-design team implemented was the use of test chips, which provided valuable insight into the impact of random and systematic variations and aided in the development of design strategies to reduce or eliminate them. As a result, the team was able to accelerate its 40-nm-development methodology.

Altera's Stratix IV 40-nm-FPGA design team is located in San Jose, CA; Penang, Malaysia; and Toronto.

ANALOG ICs

AD9272 eight-channel ultrasound receiver (Analog Devices)



The AD9272 AFE (analog front end) conditions and digitizes the sensors in ultrasound machines. As such, it includes a VGA (variable-gain amplifier) and an AAF (anti-aliasing filter) in front of an ADC. It integrates eight sets of these components to allow the conditioning of eight ultrasound sensors. The device also includes a low-noise amplifier for each channel. The input noise is 0.85 $nV/\sqrt{Hz}$, and input-noise current is 1 $pA/\sqrt{Hz}$. Outputs are LVDS (low-voltage differential signaling). The part can sample at 80M samples/sec. Power consumption is 195 mW/channel at 40M samples/sec. This power consumption includes the low-noise amplifiers that are external in most other designs. You program the part using an SPI (serial-peripheral interface).

ADCs AND DACs

SAM1610/05/00 12-bit ADCs (Samplify Systems)

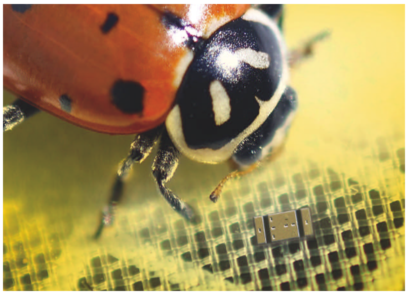
The SAM1600 family comprises the first ADCs with integrated signal compression. This novel technology reduces ADC pin count and I/O-power consumption by as much as 75% for high-channel-density applications, such as ultrasound, 4G (fourth-generation) wireless base stations, ATE (automated test equipment), and radar/sonar receivers. The part incorporates a low-latency-compression algorithm. It enables a lossless mode as well as two near-lossless modes: one tracking a user-selected compression ratio for systems with fixed-bandwidth links and the other preserving a user-selected dynamic range in increments of 0.5 dB. The SAM1600 family has a power consumption of just 44 mW per channel. By using compression, designers significantly reduce I/O count, memory sizes, wires in cables, and PCB (printed-circuit-board) traces.

BEST CONTRIBUTED ARTICLE

"High-voltage, low-noise dc/dc converters,"
Jim Williams, Linear Technology Corp,
www.edn.com/article/CA6582859
You can make a 1-kV dc/dc converter with only 100 μV of noise.

RFICs

VMMK-2x03 RF amplifier (Avago Technologies)



The VMMK-2x03 high-performance RF amplifier comes in a 1×0.5×0.25-mm package. The amplifier's design team leveraged its knowledge in gallium-arsenide PHEMTs (pseudomorphic high-electron-mobility transceivers), frequency, dielectrics, miniaturization, ceramics, plastics, and metals to develop a breakthrough in packaging technology, resulting in a product that combines wireless-chip microminiaturization and high-frequency performance. The team's key achievement was building a small package that maintains an air cavity above the microwave circuit. The company manufactures the package in wafer form during fabrication. The economies of scale allow this approach—with no wire bonds, no assembly, and no mold—to become lower in cost as volume increases.

ASSPs

CX20562 USB speakers on a chip (Conexant)

Conexant's CX20562 speakers-on-a-chip device combines the performance of a digital/voice processor, an audio codec, and a Class D amplifier. The chip set includes stereo performance; a high-fidelity, 24-bit DAC for music rendering; a built-in, echo-free speakerphone with wideband AEC (acoustic-echo cancellation); and a noise-reduction hardware DSP. An integrated 1.2W Class D amplifier suits the CX20562 for use as the preamp for larger powered speakers. The chip set features advanced DSP algorithms for superior audio and voice quality, including BrightSound, night mode, echo-free mode, and noise reduction.

LOGIC AND INTERFACE ICs

26 series SQI (SST)

The 26 series SQI (serial-quad I/O) family consists of 4-bit, multiplexed-I/O, serial-interface flash-memory devices. With an 80-MHz operating frequency and specialized instruction set, the devices target XiP (execute-in-place) applications, allowing you to store and execute programs directly from flash memory without the need for code shadowing on an SRAM. A low pin count and enhanced serial-interface architecture make the family an ideal code-storage approach for applications in which small form factor, low power consumption, and high data rate are important. To reduce access time, the devices support 8-, 16-, 32-, and 64-byte burst-mode operation with wraparound, allowing designers to execute code in burst snippets for RAM-less applications or fill cache-line buffers for applications in which the system architecture uses pipelining to maximize bus bandwidth.

MEMORY

X-25E Extreme SATA solid-state drive (Intel)

Intel's highest-performing solid-state drive, the X-25E Extreme SATA SSD (solid-state drive) shatters performance barriers associated with traditional hard-disk drives in server/storage models and significantly lowers total infrastructure, cooling, and energy costs in storage environments ranging from midsized businesses to corporate data centers. The X-25E Extreme SATA SSD offer a seven-times-higher MTBF (mean time between failures) and more-than-10-times increased life expectancy compared with hard drives.

PROGRAMMABLE LOGIC AND FAST-TURNAROUND ASICs

Stratix IV 40-nm FPGA (Altera)

Stratix IV FPGAs are the industry's highest-density, highest-performance, and lowest-power FPGAs. The first FPGA developed at the 40-nm-process node, Stratix IV leverages proven transceiver and memory-interface technology. The Stratix IV GX variant features as many as 48 transceivers supporting data rates as high as 8.5 Gbps. The transceivers deliver excellent jitter performance and signal integrity for both backplane and chip-to-chip applications. The family incorporates a hard IP (intellectual-property) core for PCIe (peripheral-component-interconnect-express) Generation 1 and Generation 2 and supports a wide range of protocols.

EDA: DESIGN ANALYSIS

Incisive Palladium DPA (Cadence Design Systems)

Incisive Palladium DPA (dynamic-power analysis) enables design teams to run long system-level tests, empowering them to correlate performance-sensitive functions' power consumption with an acceptable user experience. DPA helps engineers quickly identify the peak and average power of SOCs (systems on chips) with "deep" software cycles at megahertz throughput for RTL (register-transfer-level) logic and gates. Leveraging Palladium III's built-in memory and RTL Compiler's power-estimation engine, Cadence provides the first high-performance, cycle-accurate integrated technology delivering full-system power analysis of hardware/software designs. Designers can use the GUI (graphical user interface) to filter information to pinpoint power-hogging blocks.

EDA: DESIGN CREATION AND ANALYSIS

Zroute chip-level router with integral DFM analysis (Synopsys)

Zroute, the new routing technology in IC Compiler, addresses emerging design and DFM (design-for-manufacturability) challenges. Zroute delivers 10-times-higher speed, higher quality of results, and better DFM capabilities than do traditional routers, as well as state-of-the-art routing technology, concurrent DFM optimizations, and multithreading throughout. Zroute uses a realistic intersecting-connectivity model. It also features a dynamic maze grid, which marries the speed of gridded routers with the flexibility of gridless ones. Zroute's architecture supports native soft-spacing rules and user-defined soft rules. By considering soft rules, antennas, vias, and wire spreading during routing rather than as a postprocessing step, Zroute achieves better manufacturability. Users report 10 to 15% fewer vias overall and 30 to 50% fewer single vias after redundant-via insertion.

EDA: PCB, FPGA, AND MIXED-SIGNAL/RF ICs

RF Design Solution (Mentor Graphics and Agilent Technologies)

Designing digital, analog, and RF mixed-technology PCBs (printed-circuit boards) requires tight integration of the physical-layout environments and their respective simulation tools to ensure optimized performance and short design-cycle times. The RF Design Solution improves productivity for the design of RF circuits, halving PCB design-cycle times. The tightly integrated product enables mixed-signal-PCB designers to design a PCB using Mentor's Expedition Enterprise or Board Station XE flows and seamlessly integrate the Mentor tools with Agilent's ADS (Advanced Design System) EDA software for RF design and simulation.

EDA: SYSTEM-LEVEL SYNTHESIS

Simscape (The MathWorks)

The new Simscape language provides engineers with a method of defining models of physical components within the Simulink environment. Using this language lets engineers control the amount of detail in their models, allowing them to create models at an application-appropriate level of fidelity. Simscape lets engineers define physical components based on implicit equations. They define the relationship between the variables through implicit equations, which are easier to formulate and program. Engineers can create and control reusable models. The Simscape language leverages Matlab, opening a new realm of modeling capabilities to engineers and providing them with the ability to model the entire multidomain physical system, including the controller, within a single simulation environment.

EMBEDDED-SYSTEM TECHNOLOGIES

Mirasol display (Qualcomm)

Mirasol, the industry's first color MEMS (microelectromechanical-system) display for mobile devices, uses the IMOD (interferometric-modulator)-reflective technology. Mirasol displays require no backlighting and therefore consume significantly less power than standard displays in portable devices. The IMOD element is a simple MEMS device that comprsies two conductive plates. One is a thin-film stack on a glass substrate; the other is a reflective membrane suspended over the substrate. An air-filled gap sits between the plates. The IMOD element has two stable states. When you apply no voltage, the plates separate, and light hitting the substrate reflects. When you apply a small voltage, electrostatic attraction causes the plates to pull together and absorb the light, turning the element black.

MICROCONTROLLERS

PIC32 32-bit microcontroller (Microchip Technology)

The PIC32 8-, 16-, and 32-bit-microcontroller line has the support of one IDE (inte-

grated development environment). The M4K core delivers 1.56-DMIPS/MHz operation through its efficient instruction-set architecture, five-stage pipeline, hardware multiply/divide unit, and dual sets of 32-core registers. The PIC32's multilayer switch fabric, or bus matrix, enables high data throughput. The DMA controller uses this switch fabric to enable DMA transactions from any location to any other location. Other innovations include a prefetch buffer with cache, a hardware-vectored interrupt controller with 64 vectors, and a full 32-register shadow set. The enhanced on-chip debugger, employing two-wire or JTAG interfaces, supports eight complex hardware breakpoints.

MICROPROCESSORS

OMAP35x applications processors (Texas Instruments)

OMAP (open-multimedia-applications platform) 35x processors include the superscalar ARM Cortex-A8 processor. The scalable line of single-chip devices provides a range of capabilities with the Cortex-A8, OpenGL ES 2.0 graphics engine, video accelerators, and TMS320C64x+ DSP, supporting the development of personal navigation systems, embedded gaming, portable medical equipment, and mobile Internet devices. Featuring four times the processing performance of the 300-MHz ARM9 core, the OMAP35x processors offer laptop-like performance, have faster clocks, and can implement instruction-level parallelism with a single processor. SmartReflex power-management technology controls voltage, frequency, and power based on device activity, modes of operation, process technology, and temperature variation. The OMAP35x evaluation module and software-development kit include software modules and a multimedia framework that works on the Linux kernel or Windows Embedded CE 6.0.

PASSIVE COMPONENTS AND SENSORS

ADXL001 iMEMS shock and vibration sensor (Analog Devices)

The ADXL001 iMEMS (integrated microelectromechanical-system) shock and vibration sensor combines size, performance, and reliability to mitigate the risk of system failure. The ADXL001 senses the early stages of component failure at frequencies as high as 22 kHz. At this bandwidth, the ADXL001 detects early bearing wear and is a more cost-effective approach to preventive maintenance. The ADXL001 is resistant to electromagnetic and radio-frequency interference and operates with an extended temperature range of −40 to +125°C, allowing its use in hazardous industrial conditions. The ADXL001 is available in a 5×5-mm ceramic package, significantly smaller than metal-can sensors. The ADXL001 allows you to continuously perform vibration monitoring without interrupting normal operation of the equipment.

BATTERY ICs

MC3467x lithium-ion-battery-charger ICs (Freescale Semiconductor)

The MC3467x family of lithium-ion-battery-charger ICs provides accurate charging current and output voltages to optimize battery life and performance for portable-consumer-electronics products. The MC34671 and MC34673 have an output-voltage accuracy of ±0.7% over temperature and a charging-current accuracy of ±5% over temperature; the MC34674 has an output-voltage accuracy of ±0.4% and a charging-current accuracy of ±8%. The MC3467x ICs can deliver as much as 1.2A of charge current to single-cell lithium-ion or lithium-polymer batteries. The battery-charger input voltage can come from an ac adapter or a USB-port power source. The input voltage of as much as 28V eliminates the need for an external input-overvoltage protection circuit, which reduces system cost and board space.

POWER-CONTROLLER ICs

ADP1043 digital-power controller (Analog Devices)

The single-chip ADP1043 digital PWM (pulse-width-modulation) digital-power controller offers a highly integrated circuit architecture and intuitive GUI (graphical user interface), providing ease of use and reduced design-turnaround time for power-design engineers working with ac/dc- and isolated dc/dc-power supplies in high-reliability server, storage, and communications-infrastructure equipment. The ADP1043's application-specific, on-chip digital-control engine works in concert with the interactive GUI and an industry-standard I^2C (inter-integrated-circuit) interface. The device integrates several discrete components onto a 5×5-mm LFCSP chip, including technology for isolated power conversion, conventional housekeeping, and monitoring. Using the ADP1043 can reduce by 10 to 15% the number of components in an ac/dc-power-supply device.

POWER ICs: DRIVERS

SA306-IHZ motor-drive IC (Cirrus Logic)

The SA306-IHZ delivers the industry's highest output current for a PWM (pulse-width-modulation) IC at 17A-peak and 5A-continuous current. The SA306-IHZ accomplishes this performance through cycle-by-cycle current limiting and an "upside-down" mounting technique that increases power dissipation by a factor of three. Cycle-by-cycle current limiting generates fault signals for the microcontroller to allow it to take the appropriate action in real time for each motor phase rather than just limiting the overall current to a safe value. You can establish a preset limit for each phase, and, in an overcurrent condition, the driver shuts down all outputs for the remainder of the switching cycle and resets the outputs with the start of the next cycle. This level of control allows for better torque control. You can flush-mount a modest heat sink to the heat tab on the package's bottom; the resulting bump in heat dissipation can go as high as 17W.

POWER ICs: GENERAL CONVERTERS

FAN5355 buck converter (Fairchild Semiconductor)

The FAN5355 allows the system chip to dynamically adjust the output voltage, lending itself to use in systems for DVS (dynamic-voltage scaling). It provides high efficiency for DVS applications and extends battery life. This buck regulator has an I^2C (inter-integrated-circuit) interface, allowing the system to dynamically adjust the digital-core-power-supply voltage based on the processor workload, reducing energy consumption. The FAN5355 offers the industry's highest-efficiency 3-MHz approach for DVS applications. It also offers the industry's best-in-class transient response.

POWER ICs: MODULES

LTM4606 μModule (Linear Technology)

The LTM4606 dc/dc regulator has an onboard input filter and noise-cancellation circuits, which achieve ultralow-noise operation, effectively reducing EMI (electromagnetic interference). The package includes the switching controller, power FETs, inductor, and supporting components. You need only a resistor, a bulk input, and an output capacitor to complete the design. The LTM4606 regulator significantly reduces switching-regulator noise by attenuating conducted and radiated energy at the source. The μModule includes the inductor, controller IC, MOSFETs, input and output capacitors, and compensation circuitry on a substrate and comes in an enclosed, surface-mount plastic package resembling an IC.

POWER SEMICONDUCTORS

TBU electronic-current limiter (Bourns)

The TBU (transient-blocking unit) integrated semiconductor-circuit-protection device addresses the conditions for catastrophic telecom faults. It blocks a transient through a current-disconnecting mechanism. The TBU allows customers to protect PCBs (printed-circuit boards) from both overvoltage and overcurrent surges. TBU protects electronic equipment within nanoseconds, essentially eliminating latency common in the circuit-protection design, limiting let-through energy. The TBU has virtually no capacitance or in-

ductance, and you can, therefore, use it in high-bandwidth applications. It has a resistive characteristic, which permits currents up to a certain level to pass unimpeded to the protected interface. In higher-current situations, the TBU switches to a high-impedance state, protecting until the surge voltage dissipates or the short-circuit reseals.

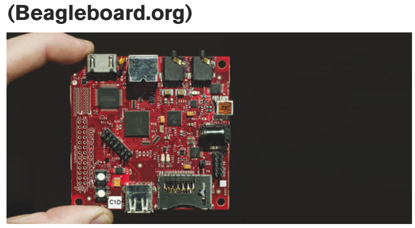
POWER SUPPLIES

BMR453 series dc/dc converters (Ericsson)

The digitally controlled BMR453 dc/dc-converter series uses a digital-control platform within the modules, freeing up real estate for improving the power density. With 96% efficiency, the BMR453 offers 396W output power with ±2% accuracy. The BMR453 modules feature a PMB (power-management-bus) interface for system connection. The net result is increased power density, greater accuracy, a higher level of control and integration within a system, and reduced through-life cost of ownership.

SOFTWARE/EMBEDDED TOOLS

Beagle Board Linux-development board (Beagleboard.org)



Offering designers and hobbyists a low-cost starting point for device development, Digi-Key, Texas Instruments, and a group of volunteers have joined forces to create an open, single-board-computer design that you can adapt to a multitude of embedded-system projects. The low-power, fanless Beagle Board module incorporates TI's recently introduced OMAP (open-multimedia-applications platform) 35x processors based on the ARM Cortex-A8 core. The processor contains 2- and 3-D graphics-acceleration capabilities plus a DSP for multimedia processing. The onboard USB interface for downloading the software from a laptop or desktop computer also powers the module. The open-source-software-development community provides a Linux operating system for the Beagle Board.

OSCILLOSCOPES

90000A series oscilloscope (Agilent Technologies)

The 90000A series oscilloscope breaks the 1-Gbps-memory barrier. The oscilloscope combines the industry's fastest, deepest memory; the lowest noise floor; the fastest offloading speed; and the fastest hardware-triggering system. It can capture events at hardware speeds that previously were available only in software. The 90000A features three USB ports on the front panel, a 12.1-in. XGA display, and buttons conveniently spaced for easy manipulation. In addition, the 90000A uses Infiniium's software GUI (graphical user interface), making even the most complex measurements easy and understandable. The 90000A has a measure-all-edges capability, allowing for more than 100,000 measurements in less than one second.

INSTRUMENTS

RSA3000B series real-time spectrum analyzers (Tektronix)

The RSA3000B series real-time spectrum analyzers provide an FMT (frequency-mask trigger), which legacy swept-spectrum or vector-signal analyzers lack. The FMT allows the user to trigger a measurement based on the occurrence of a unique pattern of events in the frequency domain. The high dynamic range of the FMT also allows triggering on weak transient signals and ignoring strong known signals. Operating across either the 15- or the 36-MHz real-time bandwidth, the FMT reliably captures elusive RF signals or frequency abnormalities that legacy analyzers miss.

DESIGN FOR TEST, PRODUCTION TEST, AND METROLOGY

Cover-Extend technology (Agilent Technologies)

Cover-Extend technology is a powerful tool available to manufacturers that must access increasingly complicated PCB (printed-circuit-board) assemblies. Traditional in-circuit test methodologies require test access on these assemblies for test engineers to use test probes to carry out their ICT (in-circuit testing). However, with shrinking board geometries and an increase in the quantity and complexity of components on each board, it has become almost impossible in many cases to find access for test probes. Cover-Extend draws its strength from boundary-scan and VTEP (vectorless-test extended performance), resulting in a tool that combines the standardized, limited-access, digital stimulus capability of boundary scan with the vectorless simplicity of VTEP. Cover-Extend simplifies design work and reduces board geometries. In addition, Cover-Extend enables more extensive electrical tests with fewer test resources.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BY DAVID DIVINS • INTERNATIONAL RECTIFIER

Use alternative approaches to evaluate dc/dc synchronous buck converters

LINEAR SYSTEMS, ONLINE TOOLS, AND FULL SIMULATIONS HELP YOU ANALYZE YOUR DESIGNS.

A number of methods exist for dc/dc-converter analysis. The one you choose depends on your proficiency as an engineer, the circuit requirements, and the availability of software tools. Before going into the analysis, however, you need to understand the makeup of these circuits, which are linear systems with feedback (**Figure 1**). You model them as classical feedback systems with transfer functions relating the output voltage to the reference voltage. You start by representing a generalized dc/dc regulator:

$$\frac{V_{OUT}}{V_{REF}}=\frac{G(s)}{1-H(s)\times G(s)},$$

where V_{OUT} is the output voltage, V_{REF} is the reference voltage, G(s) is feedforward, and H(s) is the direct feedback.

Taking a typical buck regulator circuit (**Figure 2**), you solve for G(s): $G(s)=D(s)\times G_P(s)$. You then derive the circuit-component values for optimum dynamic performance by using standard equation-manipulation and control-system theory. You can then rearrange **Figure 1** and rewrite the transfer function. This step allows you to determine the output voltage's and duty cycle's response to a load-current step. You can easily vary component values to determine their effect on the circuit's output. Tools that facilitate such mathematical manipulation include The MathWorks' (www.mathworks.com) Matlab and Simulink, open-source Maxima (http://wxmaxima.sourceforge.net), Gnu's Octive (www.gnu.org/software/octave/download.html), Scilab's (www.scilab.org) Scilab/Scicos, and PTC's Mathcad (www.ptc.com/products/mathcad).

You can design the compensation network and dynamic re-

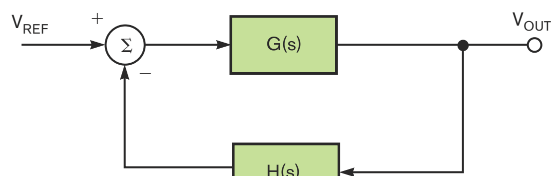

Figure 1 A dc/dc regulator is a linear system with feedback. You model it as a classical feedback system with a transfer function relating the output voltage to the reference voltage.

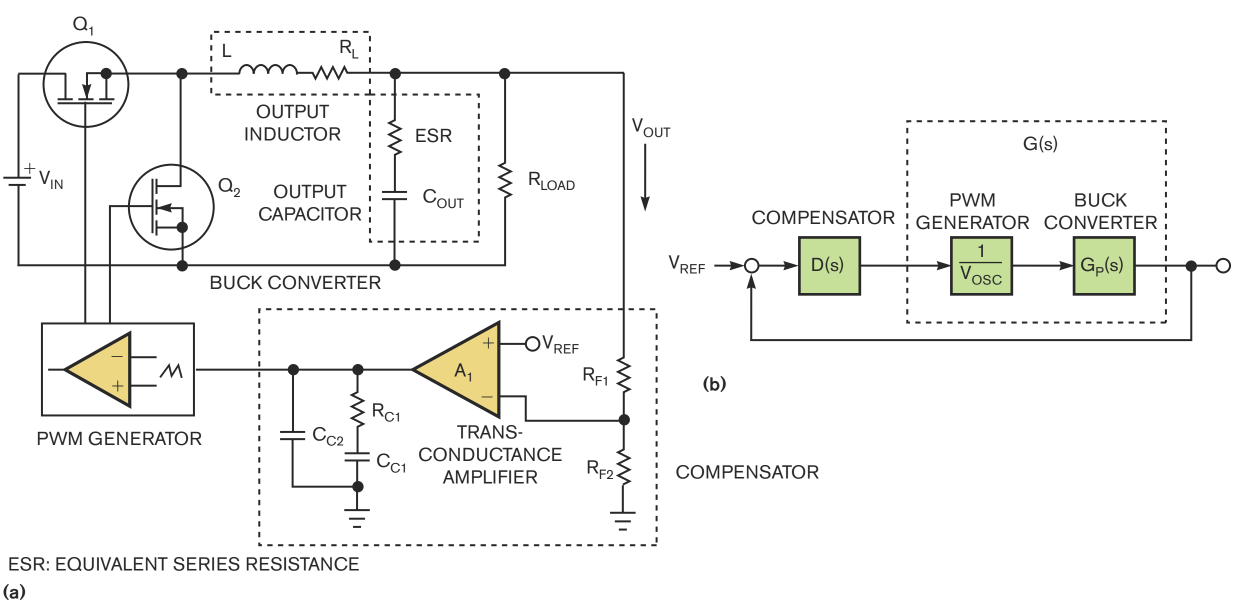

Figure 2 Taking a typical buck regulator circuit—shown here in circuit (a) and block-diagram (b) form—you solve for G(s): $G(s)=D(s)\times G_P(s)$.

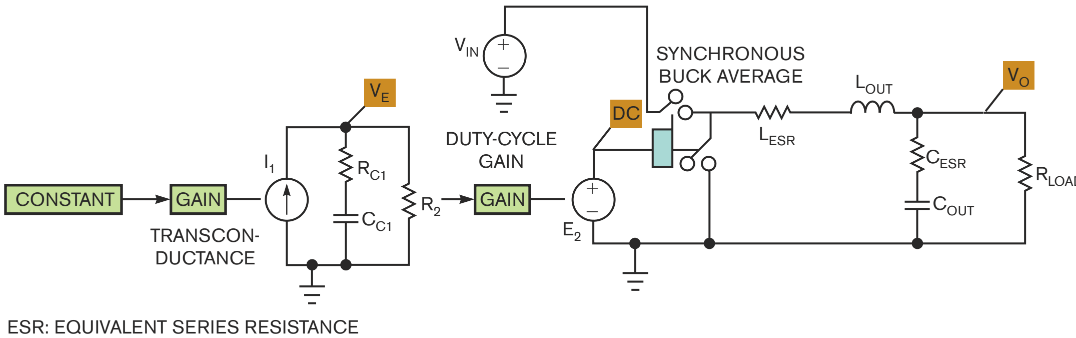

Figure 3 Simulation software allows you to represent a dc/dc converter as an open-loop state-average model.

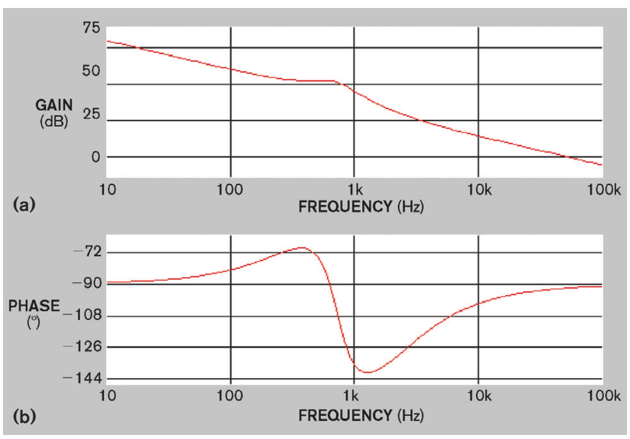

Figure 4 Using the design equations in the vendor's data sheets, you calculate the component values for gain (a) and phase (b); the simulator then validates the performance of the circuit, presenting it as an open-loop bode plot.

sponse of a dc/dc converter using a linear-system approach. This approach requires an understanding of control-system analysis and design and of Laplace-transform techniques. The most mathematically rigorous approach, linear analysis provides a good system model but no detailed circuit-performance information. Using the linear-system-analysis approach allows you to quickly simulate the open-loop response from the transfer function or block diagram to determine system stability—that is, phase and gain margins. The approach uses controller vendor provided transfer functions and block diagrams and data sheets or application notes. On the other hand, this approach does not allow you to analyze circuit behavior, such as inductor ripple current, output-voltage ripple, and efficiency. It also forces you to rewrite transfer functions or reconfigure block diagrams for each response type.

ONLINE TOOLS

As an alternative to the linear-system approach, vendors of dc/dc-controller ICs provide online design tools targeting their controller offerings and providing various types of analysis. Because these tools target specific components, vendors have optimized the tools to provide fast and accurate results for the various analyses for designing and implementing a dc/dc regulator. You can use these tools to visualize control-loop compensation and dynamic performance, such as step response, ripple voltage, ripple current, and efficiency. Vendors also help you choose the accompanying MOSFETs the converter uses. These tools use custom routines and Spice as their mathematical engines.

This approach requires little mathematical manipulation on the user's part. Usually, the user needs only to derive the compensation-component values and enter data into an online form. Some vendors' online tools aid you in deriving the compensation-component values. Each vendor formats its tools in a unique way, providing a different view of the same prob-

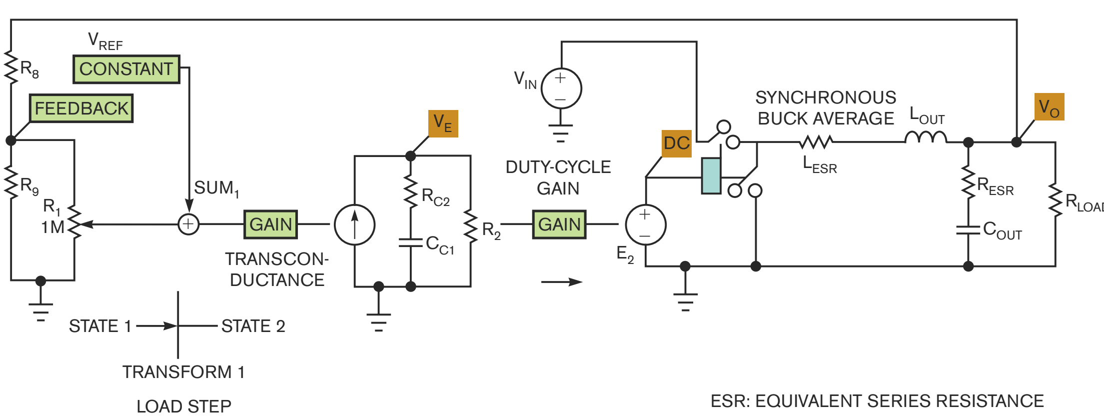

Figure 5 Software allows you to model a dc/dc converter in a closed loop using a state-average model.

lem. Companies including Fairchild Semiconductor (www.fairchildsemi.com), International Rectifier (www.irf.com), Intersil (www.intersil.com), National Semiconductor (www.national.com), and Texas Instruments (www.ti.com) provide such tools as offline Spice simulators, MOSFET-selection guides, reference-board designs and support, online simulation, and Spice models. Each vendor has a method for providing design aid to the engineering community. Vendors that use online tools control the analysis types and provide accurate simulation results. This approach provides an alternative to manual calculations and offline simulation. As with linear-system analysis, online tools have both pros and cons.

On the plus side, the vendors of these tools validate them, they are easy to use, they typically have associated demo boards, and they require no third-party software. On the other hand, they provide limited what-if analysis and minimal parameter-variation capability. They also don't allow you to change the circuit topology from the one that the vendor presents.

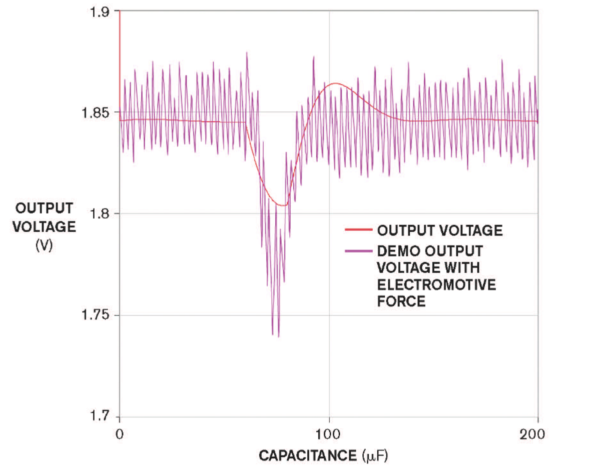

Figure 6 The results of a state-average simulation correlate well with the measurements from a demo board. The simulation does not show the converter output ripple, however.

USING FULL-CIRCUIT SIMULATION

Engineers have used circuit simulation for more than four decades for IC design and for 25 years for power-electronics design. The tool of choice has long been Spice, which is still the de facto standard in circuit simulation and analysis. Other high-power circuit simulators are available, however, including Synopsys' (www.synopsys.com) Saber, Mentor Graphics' (www.mentor.com) Eldo and SystemVision, Ansoft's (www.ansoft.com) Simplorer, and Cadence's (www.cadence.com) Spectre. The value of offline simulation and analysis is its flexibility in circuit topology and postprocessing analysis. Simulation allows for the same types of analysis as linear-system analysis and vendors' online tools. However, this approach also allows you to perform a number of other valuable analyses, such as state-average modeling. This type of modeling combines the design techniques and speedy results of control-system analysis. State-average modeling allows for both open-loop and control analysis in the circuit domain instead of the linear-system domain.

You can create a model of a dc/dc-POL (point-of-load) converter, which includes the gain of the transconductance feedback amplifier, the compensation components, and the fixed duty-cycle-conversion gain. You can then create a state-average model of the PWM (pulse-width-modulation)/power stage, the output filter, and the load (**Figure 3**). The state-average model for the PWM/power stage simplifies and linearizes the circuit for fast simulation and allows for linear-system analysis.

You can start with the transfer function for the state-average model: $V_{OUT} = D \times V_{IN}$. Then, using the design equations in the vendor's data sheets, you calculate the component values. The simulator can then validate the performance of the circuit by running an ac analysis (**Figure 4**). Full-circuit simulations also allow you to create a macro model of a closed-loop dc/dc-POL circuit using a state-average model (**Figure 5**).

The simulation results from a state-average model can produce good steady-state and dynamic results when you compare them with those from an actual circuit (**Figure 6**). The results show dynamic information but not ripple information. State-average models provide 20-times-faster simulation than does a PWM simulation. This method of dc/dc-converter analysis also has benefits and drawbacks. For example, it offers freedom from circuit-topology constraints and postprocessing analysis. It also offers both state-average and full-PWM modeling. On the other hand, not all vendors' models are available, and the state-average model has simulation-convergence issues and requires a knowledge of macro modeling.

With the maturity of simulation as a design and validation tool and the emergence over the past few years of online tools, you have a plethora of methods for analyzing dc/dc converters. Both system- and circuit-simulator tools can also play important roles because of their inherent flexibility and their history of use. In addition, engineers have a good understanding of dc/dc-POL converters, and there is much available information on them. So, no matter which design tack you take, a suitable tool is available to accomplish the job. **EDN**

AUTHOR'S BIOGRAPHY

David Divins is a senior applications engineer at International Rectifier, where he has worked for eight years. In his current position, he designs discrete power components and analog ICs into industrial and automotive applications. He has a master's degree in electrical engineering from the State University of New York—Binghamton. His personal interests include circuit simulation and analysis.

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Simple method uses PSpice for Thevenin-equivalent circuits

David Karpaty, Analog Devices Inc, Wilmington, MA

Thevenin- and Norton-equivalent circuits, among the most fundamental circuit-analysis theorems, can be useful for determining a load resistance for maximum power transfer, simplifying circuit models, and a variety of other analysis techniques. Unfortunately, calculating the Thevenin voltage and resistance can become difficult as circuit complexity increases. **Figures 1**, **2**, and **3** illustrate a simple method for obtaining the Thevenin voltage and resistance—and, subsequently, the Norton equivalence—with the aid of simulation. First, you choose an arbitrary load resistance, R_{LOAD}—2 kΩ in this example—and run the simulation to get the current through the load resistance. Next, you remove the load resistance and simulate the open-circuit voltage across nodes A and B to obtain the Thevenin voltage. You obtain the Thevenin resistance from those two values.

The Thevenin-equivalent circuit must produce the same current through the load. The total resistance in the Thevenin circuit is $R_{TOTAL}=(V_{TH}/I_{LOAD})=(374.095\text{ mV}/60.301\ \mu\text{A})\simeq 6.203\text{ k}\Omega$, where R_{TOTAL} is the total resistance. Therefore, the Thevenin resistance is simply $[(V_{TH}/I_{LOAD})-R_{LOAD}]=(R_{TOTAL}-R_{LOAD})=6.203\text{ k}\Omega-2\text{ k}\Omega\simeq 4.203\text{ k}\Omega$, where V_{TH} is the Thevenin voltage and I_{LOAD} is the load current.

Figure 4 shows the Thevenin-equivalent circuit, and **Figure 5** shows the Norton-equivalent circuit. Note that, because the net current through the load flows to the left, the positive Thevenin terminal is grounded.

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Without the aid of simulation, you can calculate $V_{THEVENIN}$ and $R_{THEVENIN}$ as follows. The array for the loop currents in **Figure 2**, assuming a clockwise current flow in each loop, gives the current through the load resistance (**Equation 1**).

$$\begin{bmatrix} +(6k)I_1 & -(2k)I_2 & -(0)I_3 & -(2k)I_4 & -(0)I_5 & -(0)I_6 \\ -(2k)I_1 & +(9.5k)I_2 & -(2k)I_3 & -(0)I_4 & -(2k)I_5 & -(0)I_6 \\ -(0)I_1 & -(2k)I_2 & +(15k)I_3 & -(0)I_4 & -(0)I_5 & -(3)I_6 \\ -(2k)I_1 & -(0)I_2 & -(0)I_3 & +(4k)I_4 & -(2k)I_5 & -(0)I_6 \\ -(0)I_1 & -(2k)I_2 & -(0)I_3 & -(2k)I_4 & +(14k)I_5 & -(2k)I_6 \\ -(0)I_1 & -(0)I_2 & -(3k)I_3 & -(0)I_4 & -(2k)I_5 & +(17k)I_6 \end{bmatrix} \begin{bmatrix} 1V \\ 0V \\ 0V \\ 5V \\ -2V \\ 2V \end{bmatrix}. \quad (1)$$

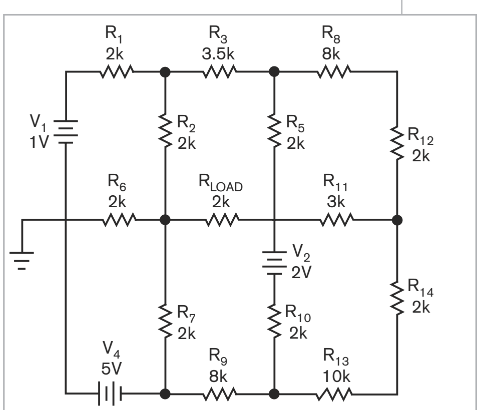

Figure 1 To calculate Thevenin-equivalent circuits, you first choose a load resistance–2 kΩ in this circuit.

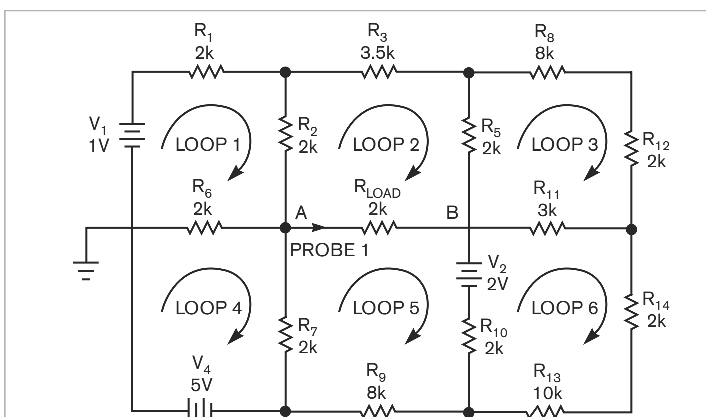

Figure 2 The simulation for current through the load resistance yields −60.3 μA.

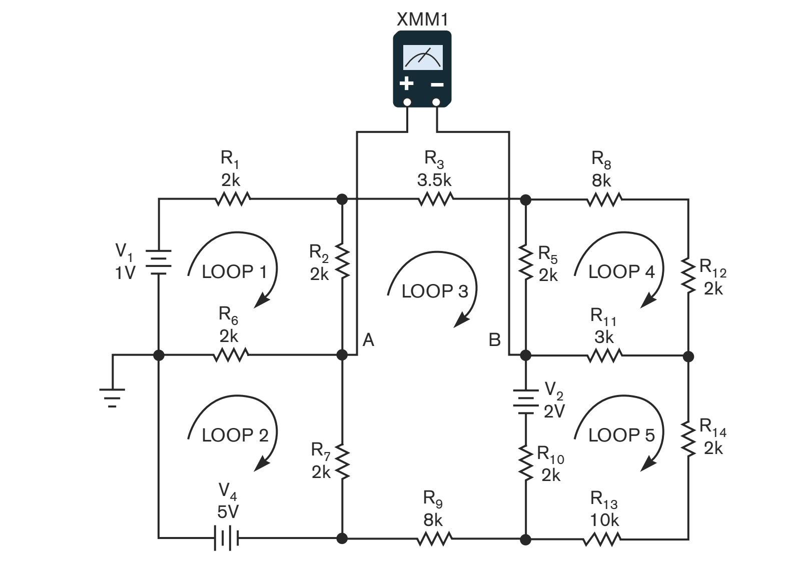

Figure 3 The simulation for the open-circuit voltage yields approximately −374 mV.

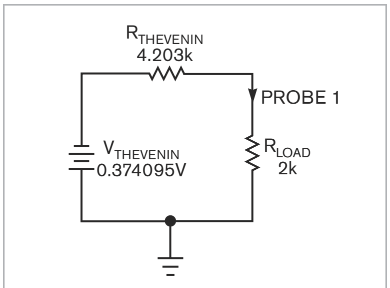

Figure 4 In the Thevenin-equivalent circuit, current flows to the left, so the $V_{THEVENIN}$ terminal is grounded.

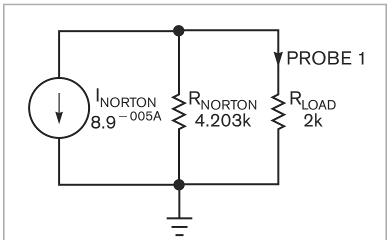

Figure 5 In the Norton-equivalent circuit, R_{NORTON} is 4.203 kΩ.

From **Equation 1**, you can calculate I_2 and I_5: $I_2 \simeq 217.77$ μA, and $I_5 \simeq 157.47$ μA. Thus, $I_2 - I_5 \simeq 60.3$ μA, assuming a leftward flow through the load resistor.

You calculate the array for the loop currents in **Figure 3** without the load resistance, as **Equation 2** shows. From **Equation 2**, you can calculate the following currents: $I_1 \simeq 807.92$ μA, $I_2 \simeq 1.744$ mA, $I_3 \simeq 179.87$ μA, $I_4 \simeq 53.64$ μA, and $I_5 \simeq 148.27$ μA.

$$\begin{bmatrix} +(6k)I_1 & -(2k)I_2 & -(2k)I_3 & -(0)I_4 & -(0)I_5 \\ -(2k)I_1 & +(4k)I_2 & -(2k)I_3 & -(0)I_4 & -(0)I_5 \\ -(2k)I_1 & -(2k)I_2 & +(19.5k)I_3 & -(2k)I_4 & -(2k)I_5 \\ -(0)I_1 & -(0)I_2 & -(2k)I_3 & +(15k)I_4 & -(3k)I_5 \\ -(0)I_1 & -(0)I_2 & -(2k)I_3 & -(3k)I_4 & +(14k)I_5 \end{bmatrix} \begin{bmatrix} 1V \\ 5V \\ -2V \\ 0V \\ 2V \end{bmatrix}. \quad (2)$$

Thus, $V_A = -V_4 + [(I_2 - I_3) \times R_7] \simeq -1.8719V$, where the net current flows downward. Further, $V_B = [(-V_4 + (I_3 \times R_9)) + ((I_3 - I_5) \times R_{10}) + V_2] \simeq -1.498V$, where the net current in R_{10} flows downward. Thus, $V_{THEVENIN} = V_A - V_B \simeq -374$ mV, and you can calculate $R_{THEVENIN}$ according to the previous description. EDN

DAC and flip-flops form constant-current source

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

The Analog Devices (www.analog.com) AD5422 16-bit serial-input DAC lets you program for a voltage output or a current output. To communicate with the DAC and produce a variable output, you need a data SERDES (serializer/deserializer). If your design needs a constant 4-mA output, however, you can program the device with two flip-flops and test it with S_1, a mechanical pushbutton switch (**Figure 1**).

The AD5422's programming uses a 24-bit word in which the upper eight bits form an address for a control register and the lower 16 bits set the DAC's output range, slew-rate step, and slew-rate clock (**Table 1**, pg 52). Programming a 24-bit 0101 ... 01 pattern into the AD5422 sets it to the bottom of the simultaneously selected current range, 4 to 20 mA at the output-current pin (Pin 19). The AD5422's internal shift-register data moves into the data register at every low-to-high transition of the latch signal (Pin 7). The device interprets this alternating bit sequence as a control command during the 23rd time you press and release the switch after IC_1's power-up. After that sequence, the SCLK signal can remain idle (**Figure 2**).

Flip-flop FF_1, configured as a familiar divide-by-two counter, produces the desired alternating sequence. Manually pressing and releasing the pushbutton switch, you cause the generation of an SCLK signal. You must use a debounc-

DESIGN NOTES

Upgrade Your Microcontroller ADC to True 12-Bit Performance

Design Note DN463

by Guy Hoover

Introduction

Many 8-bit and 16-bit microcontrollers feature 10-bit internal ADCs. A few include 12-bit ADCs, but these often have poor or nonexistent AC specifications, and certainly lack the performance to meet the needs of an increasing number of applications. The LTC®2366 and its slower speed versions offer a high performance alternative, as shown in the AC specifications in Table 1. Compare these guaranteed specifications with the ADC built into your current microcontroller.

This family's DC specifications are equally impressive. INL and DNL are guaranteed to be less than ±1LSB. Operating from a single 2.5V, 3V or 3.3V supply, the current draw on these parts is a maximum of 4mA during a conversion. This can be reduced to less than 1µA by placing the part into SLEEP mode during periods of inactivity, which greatly reduces the average supply current at lower sample rates.

These ADCs are available in tiny 6-lead and 8-lead TSOT-23 packages. The 8-lead devices have adjustable V_{REF} and OV_{DD} pins. The adjustable V_{REF} pin allows the input span to be reduced to 1.4V. This, combined with the high ADC input impedance, can eliminate the need for gain or buffer stages in many applications. The OV_{DD} pin, which controls the digital output level, can be adjusted from 1V to 3.6V, simplifying communication with different logic families. For applications that do not require an adjustable reference or adjustable output levels, the 6-lead device with $V_{REF} = OV_{DD} = V_{DD}$ should suffice.

The SPI interface requires only three wires to communicate with the microcontroller, keeping the overall solution size small in low power, high speed applications.

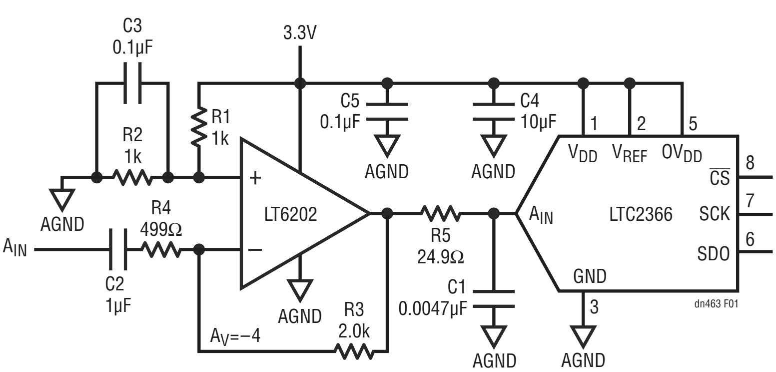

Figure 1. Single Supply AC-Coupled Amplifier Level Shifts Input for Maximum Dynamic Range

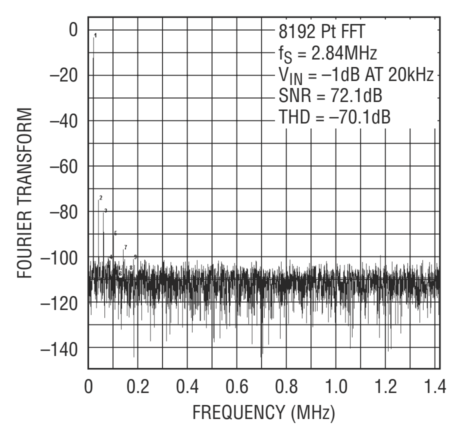

Figure 2. FFT Shows Low Noise and Distortion of Figure 1 Circuit

Application Circuits

Figure 1 shows a single supply AC-coupled amplifier driving the LTC2366. This circuit is useful in applications where the sensor output level is too low to achieve full SNR performance from the ADC. The output of the LT®6202 swings rail-to-rail. This feature maximizes the circuit's dynamic range when the op amp output is level shifted to the center of the ADC's swing. The FFT of Figure 2 demonstrates the low noise and distortion of this circuit.

In Figure 3, a single supply DC amplifier with a programmable gain of 0 to 4096 drives the LTC2360. With a maximum offset of 10µV and a DC to 10Hz noise of 2.5µV_{P-P}, the LTC6915 is a good choice for high gain applications. This circuit is useful for very low level signals or for applications with a wide range of input levels.

Conclusion

The 12-bit ADCs in the LTC236x family guarantee AC specifications that most built-in microcontroller ADCs cannot meet, thus improving performance when used in place of on-chip ADCs. The LTC236x family is easily interfaced to most microcontrollers via its SPI interface. A wide range of sample rates, an external reference pin and a separate OV_{DD} pin provide additional flexibility.

Table 1. LTC236x ADC Family AC Specifications

PART NUMBER	SAMPLE RATE	SINAD	SNR	THD	FULL LINEAR BANDWIDTH
LTC2366	3Msps	68dB (Min)	69dB (Min)	–72dB (Max)	2.5MHz (Typ)
LTC2365	1Msps	68dB (Min)	70dB (Min)	–72dB (Max)	2.0MHz (Typ)
LTC2362	500ksps	72dB (Typ)	73dB (Typ)	–85dB (Typ)	1.0MHz (Typ)
LTC2361	250ksps	72dB (Typ)	73dB (Typ)	–85dB (Typ)	1.0MHz (Typ)
LTC2360	100ksps	72dB (Typ)	73dB (Typ)	–85dB (Typ)	1.0MHz (Typ)

D3	D2	D1	D0	GAIN
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	4
0	1	0	0	8
0	1	0	1	16
0	1	1	0	32
0	1	1	1	64
1	0	0	0	128
1	0	0	1	256
1	0	1	0	512
1	0	1	1	1024
1	1	0	0	2048
1	1	0	1	4096
1	1	1	0	4096
1	1	1	1	4096

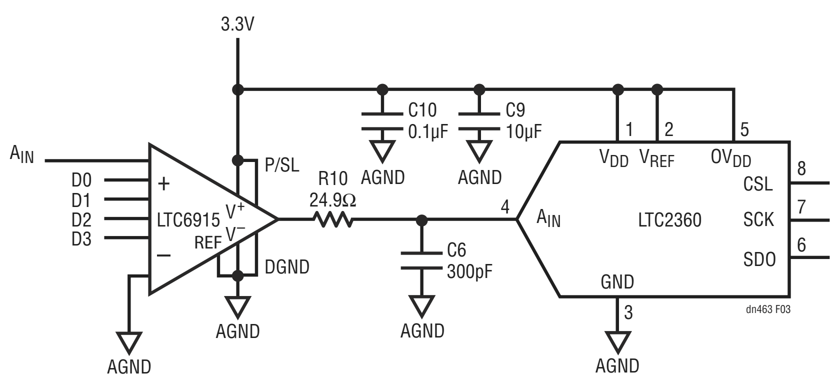

Figure 3. Single Supply DC Amplifier Provides Programmable Gain from 0 to 4096

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er because the circuit requires a clean logic signal for SCLK with level transitions that do not exceed a few 10s of nanoseconds. FF_2 acts as an asynchronous set/reset flip-flop that debounces the signal from the button.

For the circuit to work properly, the active low-to-high transition of the latch signal must occur at least 13 nsec after the low-to-high transition of SCLK. You can fulfill this requirement by using the SN74HC74-class flip-flop. The Q output of FF_1 in IC_2 connects to the SDIN input of IC_1. The level transitions at the SDIN input must have preset and hold times of at least 5 nsec with respect to low-to-high transitions of the SCLK signal. You can derive the supply voltage of 5V for the pull-up resistor at the $\overline{\text{FAULT}}$ output of IC_1 (Pin 3) for IC_2 from the AD5422's precision 5V reference. The tiny current surges due to loads appear at the initializing state, at clocking in the control word to IC_1, or in a faulty state when the open-drain $\overline{\text{FAULT}}$ output of IC_1 is active. Fortunately, either the output current (Pin 19) is not yet flowing, or an overtemperature condition or an excessive value of the load resistor causes external damage to the precision of this current. In either case, the external loading of the internal reference

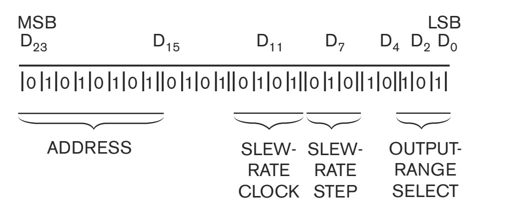

Figure 2 Although the control-command sequence is at least 23 clock pulses wide, you can easily generate the alternating bit pattern.

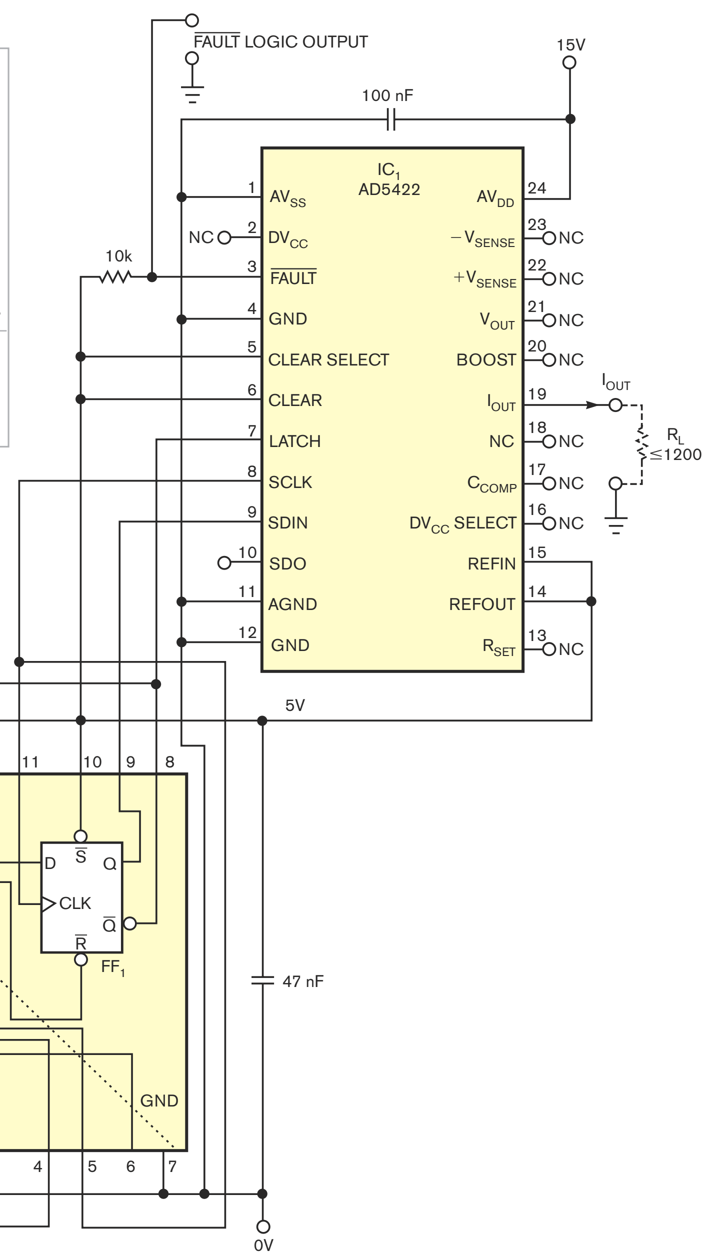
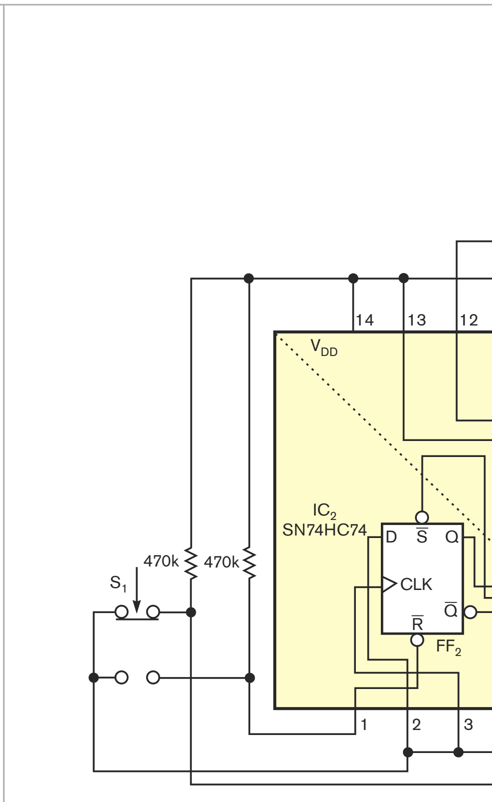

Figure 1 After you press and release S_1 23 times, the DAC produces a constant-4-mA-current output.

source, which is no more than a few 10s of microamperes, is harmless to the precision of the reference source.

By connecting a high-precision, 100Ω resistor between the I_{OUT} pin and ground and generating 23 clock pulses, you can measure a voltage of 0.400xV on this resistor, where x≤4, confirming the high-precision, constantly flowing current of 4 mA. The actual full-scale-range error of IC_1 is far below its guaranteed worst-case value of ±0.3% full-scale-range error (**Reference 1**). Hence, you must divide the observed relative error of the 4-mA current, with a value not exceeding 0.1%, by four because the current scale is 20 mA−4 mA=16 mA. The total full-scale-range error of the DAC in this case is thus less than 0.1%/4, or 0. 025%. By using the constant-current source employing a monolithic DAC, you get high resolution, negligible sensitivity to temperature, immunity to supply-voltage variations, and high initial accuracy. Current-output DACs also exhibit output resistance in the 10s of megohms.

This circuit uses S_1 to generate the SCLK signal for testing purposes only. For power-on-the-go applications, you can use a free-running clock with a frequency as high as 200 kHz. You can supply the pull-up resistor at the $\overline{FAULT}$ output and IC_2 from the AD5422's DV_{CC} pin.EDN

TABLE 1 EFFECTS OF THE SINGLE BITS OF THE CONTROL COMMAND

$D_2D_1D_0$=101	Selects 4- to 20-mA current range
D_3=0	Disables daisy-chain operation
D_4=1	Enables slew-rate control
D_7 to D_5=101	Selects slew-rate size of 4 LSB
D_{11} to D_8=0101	Selects slew-rate update-clock frequency of 69.444 kHz
D_{12}=1	Enables outputs
D_{13}=0	Deactivates external-resistor pin
D_{14}=1	Increases output voltage by 10%
D_{15}=0	Concerns only the voltage output

REFERENCE

1 "Single Channel, 12/16-Bit, Serial Input, Current Source and Voltage Output DACs, AD5412/AD5422," Analog Devices, 2008, www.analog.com/static/imported_files/data_sheets/AD5412_AD5422.pdf.

Convert negative inputs to positive outputs

Shane Chang and Budge Ing, Maxim Integrated Products, Sunnyvale, CA

You can obtain a precise, positive-output voltage from a negative-voltage supply with a boost converter and a linear regulator. The input and output capabilities of the circuit in **Figure 1** depend on the allowable I/O voltages of IC_1 and IC_2. In this case, IC_1 and IC_2 convert a −5V input voltage to a 3.3V output voltage.

IC_1 is a boost converter that accepts −5V when its V_{CC} pin connects to common ground—that is, the ground of the negative-power-supply input. Voltage divider R_1/R_2 at IC_1's output provides feedback that sets the output voltage 10.5V above IC_1's ground pin. With the feedback-threshold voltage factory-set to 1.226V, you can choose values for R_1 and R_2 using this **equation:** $(1.226V/R_2)\times(R_1+R_2)=10.5V$. Current through R_1 and R_2 should be at least 2 μA. The IC_1 output, which is IC_2's input, is 10.5V higher than −5V, which is 5.5V with respect to common ground.

IC_2, a linear regulator whose ground pin connects to the common ground, accepts input voltages as high as 6.5V. Its output is factory-set at 3.3V. **Figure 2** shows the output voltage versus the output current for the circuit in **Figure 1** with input voltages of −4.5, −5, and −5.5V.EDN

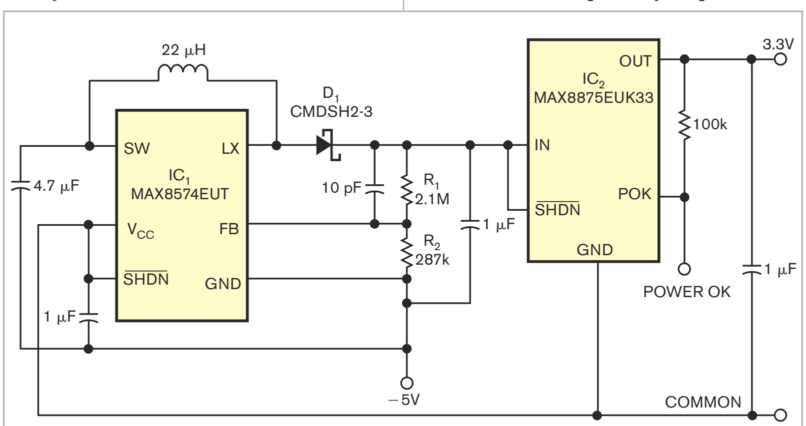

Figure 1 A two-IC circuit converts a −5V input to a 3.3V output.

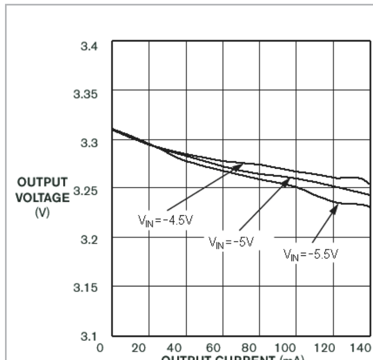

Figure 2 The circuit's output voltage drops as current increases. Plots indicate source voltages of −4.5, −5, and −5.5V.

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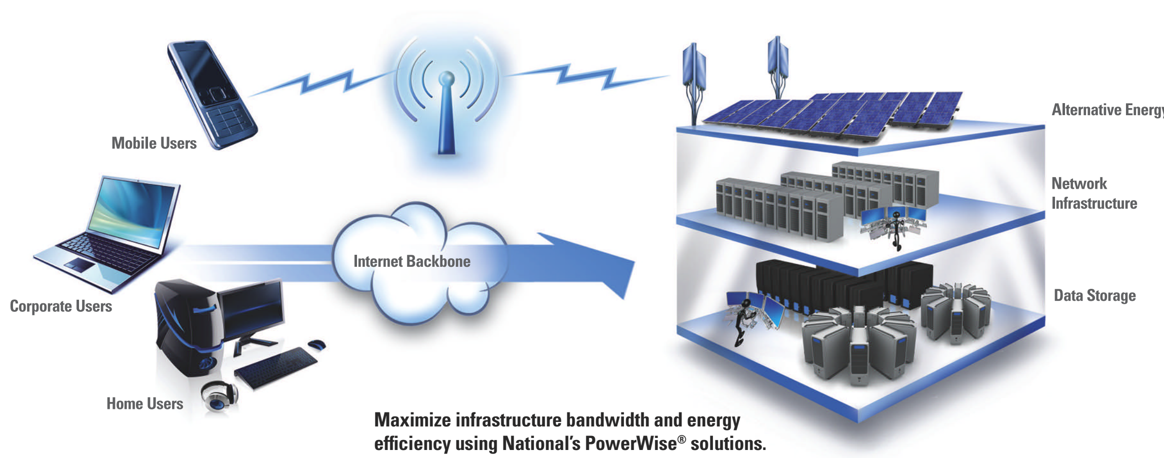

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Weathering the Storm

HOW DISTRIBUTORS HELP CUSTOMERS NAVIGATE ROUGH SEAS

INSIDE:

INCLUDING: THE TOP 25 ELECTRONICS DISTRIBUTORS LIST

"**WEATHERING THE STORM**" continues with additional coverage **online**. "Shedding some light on the stimulus package" takes a look at how distributors are seeking opportunities in infrastructure and energy provisions. To access, go to **www.edn.com/top25distributors**.

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225 Wyman Street, Waltham, MA 02451
Phone: (781) 734-8000
www.edn.com

EDN Worldwide

Russ Pratt, *Publisher*
Phone: 781-734-8417
Fax: 781-734-8070
rpratt@reedbusiness.com

Judy Hayes, *Associate Publisher*
judy.hayes@reedbusiness.com

Regina Twiss, *Project Manager*
reginatwiss@comcast.net

Barbara Jorgensen, *Special Issue Editor*

Ray Kavula, *Art Director*

A LETTER FROM THE EDITOR

PROVIDING STABILITY during turbulent times

By **Barbara Jorgensen**

It's tempting to compare the current economic crisis with the most recent and still-memorable downturn of 2001. The reality is the two are nothing alike. As one executive puts it: "In 2001, at least it felt like we had some control over the situation. The problem was largely of our own making, and we knew what we had to do. It wasn't pretty—but we did it."

The current downturn is clearly deeper and more widespread than past recessions. The "whys" have been analyzed to death, and the best economic minds in the world still can't answer "what's next?" The only thing distributors know for sure is that their future will be tied to their customers.

Customers aren't turning to their authorized distributors for a silver bullet or a new business model; they are looking for more of the same services they already rely on. At the top of the list: inventory management. Nobody—supplier or OEM—wants to be holding parts right now. The channel's ability to hold and manage inventory is enabling customers to put off purchases until the last minute. Reasonable fluctuations in these orders can be buffered by distributors. The channel breaks down bulk inventory to get customer orders as precise as possible. Authorized distributors manage returns of unused products, and the channel's credit services allow customers to pay for inventory over time.

Suppliers continue to leverage the channel's reach into a broad customer base. As suppliers cut back on sales and engineering staff, they turn to the channel to support sales efforts and advise customers on the best combination of parts for a particular solution. Component makers also rely on the channel for demand information as signals from the end-market continue to be unclear. "We need to plan for our production capacity," says one supplier executive. "That's tough to do when orders are pushed out or cancellations start to build up."

During this period of cataclysmic change, consistency has become reassuring to many in the industry. The make-up of the Top 25 Distributors hasn't changed dramatically in a number of years. The channel will continue to evolve, but it's the fundamentals that will help the supply chain weather the economic storm. ■

Freelance writer Barbara Jorgensen has been covering the electronics distribution industry for nearly 20 years, most recently as a Senior Editor at Electronic Business *magazine.*


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TOP 25 North American Electronic Component

Rank	Company name	CALENDAR YEAR 2008 North American revenue (millions of $)	CALENDAR YEAR 2008 Total revenue (millions of $)	Total revenue change 2007-2008	5-year compound annual growth	Public/ private	Authorized/ independent	% OF REVENUE 2008 North America	Europe	China	India	Japan
1	**Avnet**	8,394.2	17,860.0	5%	15.0%	P	A	47.0%	34.0%	19% in Asia/Pacific		
2	**Arrow Electronics**	8,380.5	16,761.0	5%	14.6%	P	A	50.0%	32.0%	18% in Asia/Pacific		
3	**Future Electronics**[1]	3,808.7	5,441.0	4%	N/A	PR	A	70.0%	N/A	N/A	N/A	N/A
4	**Bell Microproducts**[1]	1,777.4	4,232.0	4%	N/A	P	A	42.0%	44.0%	0.0%	0.0%	0.0%
5	**Digi-Key Corporation**	776.9	983.4	4%	20.0%	PR	A	79.0%	10.0%	3.0%	1.0%	2.0%
6	**TTI Inc.**	737.5	1,250.0	9%	16.6%	P	A	59.0%	32.0%	9.0%	0.0%	0.0%
7	**Newark**[3]	665.6	679.2	8%	N/A	P	A	98.2%	0.0%	0.0%	0.0%	0.0%
8	**Nu Horizons**	513.4	789.8	0%	18.4%	P	A	65.0%	9.0%	13.0%	2.0%	0.0%
9	**DAC**	488.5	493.4	2%	16.0%	PR	A	99.0%	0.0%	1.0%	0.0%	0.0%
10	**Carlton-Bates**[2,4]	385.2	385.2	3%	N/A	P	A	100.0%	0.0%	0.0%	0.0%	0.0%
11	**Sager Electronics**[1]	342.4	345.9	5%	N/A	PR	A	99.0%	1.0%	0.0%	0.0%	0.0%
12	**Allied Electronics**[2,5]	336.6	340.0	5%	N/A	P	A	99.0%	0.0%	0.0%	0.0%	0.0%
13	**Converge**[6]	311.0	311.0	N/A	N/A	PR	I	100.0%	0.0%	0.0%	0.0%	0.0%
13	**Smith & Associates**	311.0	311.0	3%	N/A	PR	I	100.0%	0.0%	0.0%	0.0%	0.0%
15	**Mouser Electronics**	256.3	298.0	30%	33.0%	P	A	86.0%	7.0%	2.0%	1.0%	1.0%
16	**Richardson Electronics**[1]	227.4	565.5	2%	N/A	P	A	40.0%	27.0%	30% in Asia/Pacific		
17	**America II Electronics**	213.3	277.0	0%	N/A	PR	I	77.0%	9.0%	5.0%	0.0%	7.0%
18	**A.E. Petsche Co.**	186.2	219.0	12%	18.0%	PR	A	85.0%	11.0%	2.0%	0.0%	1.0%
19	**Fusion**[6]	178.5	210.0	5%	8.5%	PR	I	85.0%	N/A	N/A	N/A	N/A
20	**Dependable Component Supply**[1]	164.8	270.2	5%	N/A	PR	I/A	61.0%	10.0%	23% in Asia/Pacific		
21	**PEI-Genesis**	149.3	171.6	18%	23.0%	PR	A	87.0%	10.0%	0.0%	0.0%	0.0%
22	**JACO Electronics**	133.4	177.8	-12%	N/A	P	A	75.0%	2.0%	2.0%	0.0%	0.0%
23	**Advanced MP Technology**[1]	113.1	323.2	7%	18.5%	PR	I	35.0%	25.0%	25.0%	0.0%	5.0%
24	**Master Distributors**	100.8	115.9	3%	N/A	PR	A	87.0%	4.0%	4.0%	0.0%	2.0%
25	**Bisco Industries**	91.5	93.4	6%	10.8%	PR	A	98.0%	0.4%	0.4%	0.4%	0.4%

Distributors are ranked by calendar year 2008 North American revenue.

N/A = Not available

Revenue figures are gathered from financial filings, company-provided information, and Reed Business Information estimates.

Distributors

				% OF REVENUE 2008						
Rest of world	Total employees 2008	Revenue per employee ($ thousands)	VA services	Active components	Passive, electromechanical, interconnect	Computer products/ systems	Contract manufacturing	Services	Other	Web address
0.0%	12,500	1,428.8	N/A	53.0%	8.0%	39.0%	0.0%	0.0%	0.0%	www.avnet.com
0.0%	12,700	1,319.8	N/A	68% active and passive		32.0%	0.0%	0.0%	0.0%	www.arrow.com
N/A	5,000	1,088.2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	www.futureelectronics.com
14.0%	2,000	2,116.0	54.0%	20.0%	0.0%	75.0%	0.0%	5.0%	0.0%	www.bellmicro.com
5.0%	2,000	491.7	10.0%	38.0%	55.0%	1.0%	0.0%	0.0%	6.0%	www.digikey.com
0.0%	2,155	580.0	65.0%	0.0%	100.0%	0.0%	0.0%	0.0%	0.0%	www.ttiinc.com
1.8%	1,507	450.7	22.2%	11.5%	48.1%	0.2%	0.0%	0.0%	40.2%	www.newark.com
11.0%	812	972.7	18.0%	85.0%	7.0%	8.0%	0.0%	0.0%	0.0%	www.nuhorizons.com
0.0%	775	636.6	40.0%	0.0%	100.0%	0.0%	0.0%	0.0%	0.0%	www.heilind.com
0.0%	N/A	N/A	N/A	0.0%	100.0%	0.0%	0.0%	0.0%	0.0%	www.carlton-bates.com
0.0%	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	www.sager.com
1.0%	760	447.4	N/A	3.6%	54.0%	0.0%	0.0%	0.0%	42.4%	www.alliedelec.com
0.0%	350	888.6	25.0%	70.0%	5.0%	25.0%	0.0%	0.0%	0.0%	www.converge.com
0.0%	309	1,006.5	N/A	74.0%	22.0%	4.0%	0.0%	0.0%	0.0%	www.smithweb.com
3.0%	670	444.8	N/A	33.0%	59.0%	0.0%	0.0%	0.0%	8.0%	www.mouser.com
3.0%	930	611.2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	www.rell.com
2.0%	500	554.0	6.0%	75.0%	23.0%	2.0%	0.0%	0.0%	0.0%	www.americaii.com
1.0%	340	644.1	20.0%	0.0%	100.0%	0.0%	0.0%	0.0%	0.0%	www.aepetsche.com
N/A	75	2,800.0	15.0%	70.0%	10.0%	20.0%	0.0%	0.0%	0.0%	www.fusiontrade.com
1.0%	N/A	N/A	18.0%	63.0%	35.0%	2.0%	0.0%	0.0%	0.0%	www.dependonus.com
3.0%	509	337.1	70.0%	0.0%	100.0%	0.0%	0.0%	0.0%	0.0%	www.peigenesis.com
21.0%	150	1,185.3	25%	78%	22%	0.0%	0.0%	0.0%	0.0%	www.jacoelectronics.com
10.0%	215	1,503.3	10.0%	60.0%	30.0%	5.0%	0.0%	5.0%	0.0%	www.advancedmp.com
3.0%	167	694.0	N/A	13.0%	87.0%	0.0%	0.0%	0.0%	0.0%	www.masterdistributors.com
0.4%	300	311.3	10.0%	2.0%	98.0%	0.0%	0.0%	0.0%	0.0%	www.biscoind.com

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[1] *Revenue figures and percentages are Reed Business Information estimates.*

[2] *Revenue figures are Reed Business Information estimates.*

[3] *Newark is parent company Premier Farnell's (West Yorkshire, England) main North American presence in electronic component distribution.*

[4] *Carlton-Bates is a subsidiary of WESCO Distribution.*

[5] *Allied is a subsidiary of Electrocomponents plc.*

[6] *North America revenue percentages are Reed Business Information estimates.*

DISTRIBUTOR SERVICES help keep customers afloat

CREDIT, INVENTORY AND DESIGN HELP OEMs STRETCH RESOURCES

By **Barbara Jorgensen**

The electronics supply chain hasn't yet forgotten the painful lessons of 2001 when the high-tech industry hit the skids. Eight years ago, the channel could point to unrealistic forecasts, double ordering and poor inventory management as contributors to the industry's steep decline.

Unlike 2001, however, the current economic crisis is not self-inflicted. This downturn is so widespread that all industries and markets are affected. That's cold comfort to electronics distributors, who have spent the last eight years getting their warehouses in order.

"These are very unusual times," says Eric Sussman, director of Americas distribution for connector supplier Molex Inc., Lisle, Ill. "No one seems to know where the bottom is."

Nevertheless, the electronics distribution channel has some unique opportunities in this environment. Distribution services considered standard operating procedure (SOP)—credit, inventory management and design assistance—help suppliers and customers stretch increasingly limited human and financial resources. Highly leveraged or struggling competitors provide strategic acquisition opportunities for distributors. Finally, as suppliers get bogged down by uncertain demand from their direct customers, they are transitioning more of these accounts into the distribution channel. "During the last downturn, suppliers rushed to add distributors to their channel over concerns about sales coverage and inventory," says Faris Aruri, vice president of corporate marketing for Sager Electronics, a privately held distributor based in Middleborough, Mass. "Today, manufacturers have been moving toward rationalizing their channel to a smaller, higher-quality group. It's affording [suppliers] the ability to get out of the customer service and logistics business on a broad base and focus their expertise on new product development."

Authorized distributors willing to assist their partners through these tough times stand to benefit in the long run. "These are the times that distributors develop relationships with customers that endure just beyond the short term," says Sussman. "If distributors can make the investment now, they can tie up a [relationship with a] customer with a strong set of services for a long time. It's a good time to place some bets and to lock up business."

"What we are seeing is reluctance in all elements of the supply chain to hold any inventory."

Harley Feldberg
President
Electronics
Marketing
Global
Avnet Inc.

Where credit is due

The extension of credit toward customer purchases has been a longtime practice in the channel. Many distributors bank on the possibility that today's start-up will be tomorrow's Apple or Sun Microsystems. Credit practices in the channel haven't changed in spite of the current economic crisis, according to both distributors and suppliers. "Our distributors' ability to extend credit has worked well, and, frankly, they are in that position to act as a buffer between supplier and customer," says Sussman.

Distributors are particularly willing to accommodate strategic accounts and longtime customers. "We know our customers and their character, and we have a reputation for dealing with folks that we have a good relationship with," says Sager's Aruri. In general, distributors say, customers are facing a number of difficulties: they can't pay their distributors on time, they can't take delivery of inventory that was ordered months ago, they are having cash-flow problems or they are waiting for funding. Authorized distributors are easing

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these pressures by extending payment terms, marketing inventory to other customers or returning inventory to suppliers. "Customers that are facing slowdowns or even shutdowns—we want them back when things get better," says Aruri.

Distributors' willingness to extend credit could become increasingly important to the design community as the economic crisis lingers on. Production orders—typically high volume, high mix and high cost—are the first casualties of a slowdown as OEMs cut back on manufacturing and distributors worry about the inventory liability of cancelled orders. However, design and prototype purchases—low-volume and low-dollar-value orders—will be the last to go. Suppliers and distributors are less concerned about the default or nonpayment of a $500 order than they are about a $50,000 purchase.

This is good news for small and/or design-oriented businesses. For distributors, credit decisions hinge more on a customer's ability to pay than on the overall size of the company. "Customers with strong balance sheets come in all shapes and sizes," says Craig Conrad, senior vice president at specialty distributor TTI Inc., Fort Worth, Texas.

Taking inventory

Another ubiquitous channel service—inventory management—will play a huge role in the supply chain as the economy continues to flounder. OEMs do not want to be caught holding inventory if their production orders slow or grind to a halt. Instead, OEMs are taking inventory shipments at the last possible moment. "I think one of the benefits that our company brings into the third- and fourth-tier production market is the ability to get inventory off the shelf almost immediately," says Mark Larson, president of catalog distributor Digi-Key Corp., Thief River Falls, Minn. "It allows customers to have a shorter planning cycle and avoid inventory risk."

The channel's inventory skills also work for suppliers. When customers delay orders, component suppliers have less visibility into actual—as opposed to forecast—end-market demand. Suppliers require several weeks of lead time to ramp up manufacturing and are loath to commit capacity to demand that may or may not materialize. Any uptick in demand could push lead times out or even prompt shortages. Distributors' on-hand inventory provides a safety net for suppliers: if vendors are unable to meet demand, customers can turn to the channel for components. "What we are seeing is reluctance in all elements of the supply chain to hold any inventory," says Harley Feldberg, president for Electronics Marketing Global at broadline distributor Avnet Inc., Phoenix. "Some people predict even the slightest upturn will cause some shortages."

Based on experience—electronics distributors have been in business since the 1940s—channel executives believe the industry will rebound. "One of the downstream things we will see is, at some point in time, these markets will come back," says Michael Knight, vice president of product management and supplier marketing for TTI. "There has been so much downsizing in the supply base and so much capacity taken offline that when we do see a resurgence, things will get interesting."

Thanks to the downturn of 2001, the channel has paid special attention to managing inventory. When demand dropped off in 2001, suppliers, distributors and customers were caught with excess inventory that quickly lost its value and was written off by the supply chain. Distributors have since developed or invested in sophisticated MRP systems, gained more visibility into end-market demand and are "reality checking" orders against historic buying patterns. These efforts have helped distributors get a better handle on inventory, and supply chain executives say inventory levels in the channel are currently in good shape relative to forecasts. "We are continuing to monitor the quality and mix of our inventory," says Avnet's Feldberg. "We do not believe our role in this market is to have no inventory on hand. In down markets, companies that have the ability to keep inventory will accelerate more [in an upturn] than those who are reducing inventory."

Channel players are also helping customers avoid the excess inventory that often accompanies volume purchases. "If our customer needs 499 devices that are sold in lots of 500, we will adjust our shipment to the customer's requirements," says Digi-Key's Larson. "Customers don't have to deal with any excess." This also pre-empts a customer's need to dispose of excess inventory through the gray market or other unauthorized channels.

A number of industry observers say that electronics manufacturing services (EMS) providers—companies that generally avoid distribution because of perceived higher costs—are also using the channel to manage inventory. "EMS companies don't want to be caught with inventory, and the pricing issues have become less of a factor as companies are willing to pay more as long as they don't have to hold inventory," Molex's Sussman says.

Inventory also plays a role in extending the lifespan of customers' equipment. Distributors in the maintenance repair and operations (MRO) market are proactively anticipating customers' service requirements. As more businesses defer investments in IT, manufacturing or other types of equipment, their focus shifts to keeping existing systems in tip-top shape.

"One of the benefits we bring…is the ability to get inventory off the shelf almost immediately."

Mark Larson
President
Digi-Key Corp.

MRO distributors are helping their customers plan an upgrade or repair.

"I think one of the areas a company with an extensive line card and engineering services can play a role in is maintenance," says DeWight Wallace, president of catalog distributor Newark, Chicago. Newark uses information from suppliers and field salespeople to anticipate customer MRO needs. "I think customers are clearly investing in more maintenance and repair as everybody who is dealing with the economic challenge is pushing capital spending decisions forward," Wallace says.

Designing for the times

Although distributors are typically associated with back-end (order fulfillment) services, the channel is expanding its role in front-end services such as design. "There is definitely a domino effect with the economy," says Wallace. "People are looking for alternative resources to fill in the gaps. Clearly, design is part of the entire value proposition distributors can offer." Although distributors can't tie increased design activity directly to the downturn, the channel continues to invest in engineering expertise. Overall, Premier Farnell—Newark's parent company—grew from 70 to 190 engineers globally in the last two years. "What our design support group is seeing in terms of activity they are not attributing to the downturn at this point, but these are still early days," says Digi-Key's Larson. "What we do see is, customers appear to be buying design tools, and that is a good sign."

Broadline distributors echo that sentiment. "What is encouraging is the interest and support we are seeing in what we call our design chain services," says Avnet's Feldberg. "These services revolve around the concept that one technology is connected to another. It's not just the DSP you buy—it's the interconnectivity of all parts that matters."

Avnet is demonstrating the value of such connectivity by designing reference boards that optimize component performance in a specific solution. These boards mix and match parts from suppliers that normally are considered competitors. Suppliers aren't complaining. In a typical purchase, customers might buy one chip or another but not necessarily tie the two together. In this scenario, both suppliers make a sale. "We are the matchmaker," says Feldberg. "I'd say this is an arena where we see significant interest accelerated by market conditions."

A buyer's market

Although financing for activities such as acquisition is hard to come by, companies with strong balance sheets are not ruling out the possibility. In fact, companies that have not historically been acquisitive are looking for strategic opportunities. "In Asia, we see the market losing a lot of [connector] competitors through attrition—these are tough times and many of these suppliers are small and under-capitalized," says Molex's Sussman. "Among those suppliers, companies that specialize in technologies we are interested in would be attractive to us."

"Acquisitions are always a possibility," says Newark's Wallace. "Premier Farnell has always invested in expanding internationally, and our growth will focus on new geographies." Channel executives point to Brazil, India and China as promising markets.

Globalization will continue to be a driver for highly acquisitive companies such as Avnet. "More and more of our customers are becoming global," Feldberg says. Distributors that are largely regional may be considering partnerships that will help them expand their reach.

Re-connecting the supply chain

In general, supply chain executives say the authorized channel can become more important to both suppliers and customers during the economic crisis. If supplier cutbacks include salespeople, the channel will play a larger role as a cost-effective way to reach multiple customers. If OEMs lay off engineers, distributor design services are poised to take up the slack. And, if inventory levels continue to be in balance, distributors will have the flexibility to respond to any upside (or downside) ordering trends.

Several channel executives note that continuity is becoming a significant factor in supply chain relationships as companies deal with layoffs. "Some of the larger suppliers are laying off salespeople, and there is a lack of continuity on both [supplier and customer] sides," says TTI's Knight. "It's not efficient for suppliers to train new salespeople, and, in some cases, small customers aren't getting a new salesperson assigned to them. This is an opportunity for distributors—one thing we are known for is our sales teams."

"Points of contact have definitely been affected," says Digi-Key's Larson. "Not only are customers feeling the impact, but suppliers are looking for ways to leverage distribution more."

Even though the channel has been through tough times before, the current environment will force the supply chain to become even more efficient. Distributors that provide valuable solutions to their partners now can cement those relationships for the long run. "There are going to be decisions made that will affect distributors in a positive way," Larson says. "Even though this is not the way we'd go about it, everyone will come out stronger." ■

"Customers are clearly investing in more maintenance and repair as everybody pushes capital spending decisions forward."

DeWight Wallace
President
Newark

RISING above the tide

END MARKETS THAT BODE WELL FOR THE CHANNEL

By **Barbara Jorgensen**

Within every business downturn there exist markets that are said to be recession-proof: markets, products and services that don't rise or fall based on overall economic conditions. In the current environment, few experts are using that term, but the supply chain is seeing some stability or even growth in some of the end markets it serves.

"Many of the markets we are pursuing are the same—we have been targeting these markets for some time," says Eric Sussman, director, Americas distribution, for connector maker Molex Inc., Lisle, Ill. "Transportation—non-automotive—military and medical tend to stay in this country and are more untapped [by distribution] than other industries."

These markets aren't necessarily new; they just haven't been as affected by the credit meltdown, the housing slump or lackluster consumer spending as other industries. "First and foremost, our military market is holding up extremely well," says Michael Knight, vice president of product management and supplier marketing for specialty distributor TTI Inc., Fort Worth, Texas. "Historically, since our foundation, we have been a big player in the military market. As support of the war effort advances, electronics [equipment] is so hot and heavy, military is starting to come back into play."

Authorized distribution plays a number of roles in the military supply chain. Military electronics used to be highly proprietary—products were designed for military use and military use only—and were therefore sold directly to military contractors. However, as off-the-shelf commercial electronics have improved in quality, the military has adopted these commercial parts in its systems. This is a win-win for component makers and military contractors; unlike proprietary products, commercial parts can be marketed across a broad range of customers and therefore are less prone to extreme ups and downs in military spending. If military contractors cancel an order, off-the-shelf parts can be sold into the commercial arena. The use of commercial components also ensures that military contractors have multiple sources of supply. Competition among these suppliers, in turn, drives costs down.

As an extension of their suppliers' sales force, authorized distributors play the same role in the military market as they do in other segments: inventory management, product flow and value-added services. The channel also provides a vital service in managing end-of-life (EOL) products. Military equipment has a very long lifespan, which means components may be discontinued by suppliers during the equipment's useful life. Distributors frequently buy the remaining inventory of such components from suppliers and hold them on behalf of military customers.

An adjunct to military is aerospace, which distributors are not as bullish about. "Aerospace has softened a bit," says TTI's Knight. "I think some of the reasons behind this are the Boeing strike and slower production of commercial jets." The International Association of Machinists went on strike against Boeing last fall and stayed off the job for eight weeks. The strike slowed down production and cost Boeing an estimated $2 billion in profits.

One of the most promising markets for the authorized distribution industry is medical equipment. There are a number of reasons the channel expects to see growth. First, manufacturers of medical equipment have historically built products in-house because of the stringent quality and performance requirements of medical products. Manufacturing is beginning to move into the outsourcing environment as more electronics manufacturing services (EMS) providers become qualified to build medical equipment. Although EMS has traditionally not been a big user of distribution, "someone out there is buying a lot of products from us," says Ed Smith, president,

"We are seeing a combination of demand-driven and outsourcing-driven growth in medical [electronics]."

Ed Smith
President
Electronics
Marketing
Americas
Avnet Inc.

Electronics Marketing Americas for Avnet Inc., Phoenix.

"We are seeing a combination of demand-driven and outsourcing-driven growth in medical," adds Smith. "EMS is getting more into the medical market because of start-ups, which tend to use Tier 2 and Tier 3 manufacturers. More of these are getting ISO certified and becoming more capable of handling the start-up medical companies. You still see a lot of the big [medical] companies doing well, but start-ups are doing great."

A second trend in medical equipment that favors the channel is the sheer size of and complexity of most products. Much of this equipment is designed and built in the Americas. Even with low-cost labor overseas, the time it takes to assemble a large product and to ship it from overseas offsets any cost effectiveness of labor. These products are also complex to build—they require small volumes of lots of different electronics parts (low-volume, high mix). If an engineering change order (ECO) has to be made on the manufacturing line, it takes a long time to execute the ECO if the factory and design engineer are half a world apart.

Finally, the aging population is driving investment in and sales of medical equipment. "The medical market grew for us the last few months [of 2008] even though growth contracted by about 4 percent or 5 percent," says Smith. "People will continue to age."

Medical equipment is being paired up with another technology that should fare well during the recession. "We are seeing strong prototyping and design activity in the wireless and medical areas," says Mark Larson, president of catalog distributor Digi-Key Corp., Thief River Falls, Minn. "It's still too early to get a reading on the impact of the downturn on the production side, but we are bullish based on the design. It may take a few months to see this play out."

Light-emitting diodes (LEDs) are being cited as a dependable and emerging market. LEDs have been used in the industrial channel—distribution's sweet spot—for decades. LEDs have mostly been relegated to on/off lights in computers, equipment, battery chargers and other low-volume applications. But as the technology has improved—colors are getting brighter and clusters of bulbs are being used in large-scale applications—LEDs are expanding into new markets.

It isn't a huge market yet. "When you look at growth in terms of the percentage of growth, the numbers are there," says Smith. Distributors can take advantage of breadth of product—the electronics used to drive LED products—and offer a system approach. "If you can sell the whole solution—a lot of it is mechanical work, the metal frames that hold the lights and other components—there's opportunity," he says.

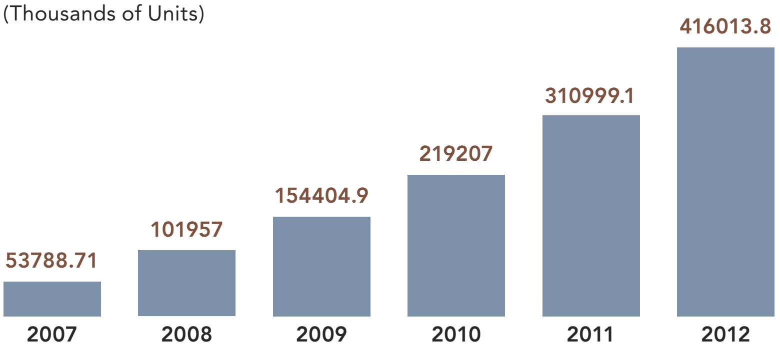
"The nice thing for distribution is there is a new customer base [for LEDs]," Smith adds. "These include sign vendors and flashlight makers. We see double-digit growth in that market and we expect that will continue for awhile."

Wireless—a term that encompasses a broad range of technologies and products—is also expected to grow at a steady pace in the near-term. Wireless has become prevalent in many end products, including PDAs, handheld computers and devices, wireless notebooks, tablet PCs, wearable computing devices, pen-based computing, infrared and wireless distribution systems, laptop computers, wireless protocol solution, healthcare applications, network storage management, security, wireless or mobile solutions software and wireless networking devices.

GLOBAL MOBILE INTERNET DEVICE MARKETS

Class device forecast with smart phones, 2007-2012

(Thousands of Units)



Source: iSuppli Corp., March 2009

Wireless technology—including mobile Internet devices and smart phones—will continue to drive electronics market growth through 2012.

"Even in the gloom and doom of the economic malaise, people will not stop talking or accessing the Internet," according to the online newsletter *RCR Wireless News*. "Wireless technology will continue to be a force-multiplier, not just in terms of enabling people and machines to talk with each other, but also with respect to advancing goals in education, health care, homeland security and governing itself."

The recession will test the mettle of many markets—not just electronics. But many see the prevalence of electronics in the home, business, military and transportation industries as evidence there will be some areas of growth. The channel aims to help its customers and suppliers capitalize on these areas—and maybe develop the next recession-proof product. ■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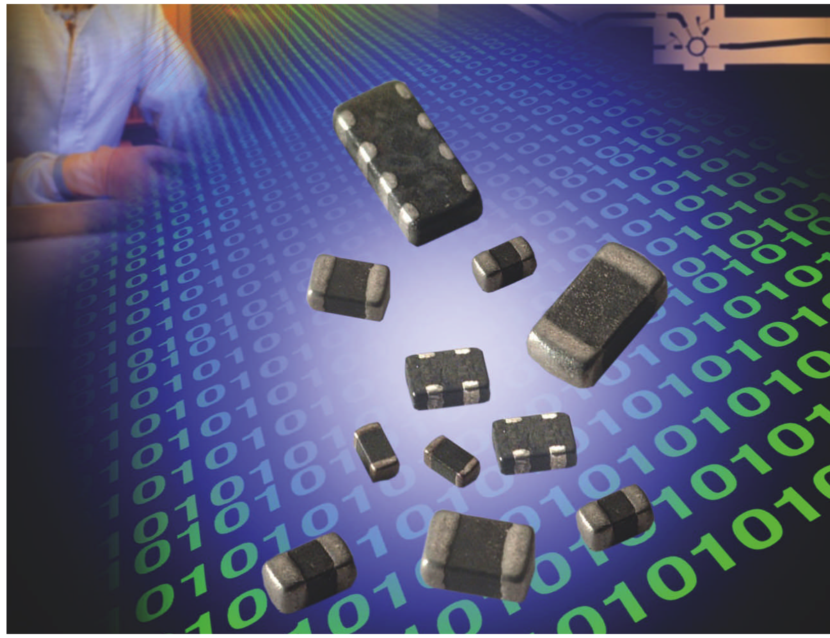


Multilayer ceramic varistors have low leakage current

Providing a 2-μA maximum leakage current, the zinc-oxide-based UltraGuard varistor series features nonlinear, bidirectional voltage-current characteristics, similar to those of back-to-back zener diodes, and an EMC (electromagnetic-compatibility) capacitor in parallel. The multilayer ceramic varistors come in discrete chips in 0402, 0603, and 0805 sizes; two-element packages come in 0405 and 0508 sizes; and four-element packages come in 0612 sizes. Suiting transient-protection applications with low-power-consumption needs, the varistors also come in low- and high-capacitance versions of 40 to 3000 pF. The UltraGuard varistor series costs 11 cents (10,000).

AVX Corp, www.avx.com

Overvoltage protectors guard against 28V faults

The MAX14527 and the MAX14528 overvoltage protectors guard low-voltage systems against voltage faults as high as 28V. Integrating a typical 100-mΩ-on-resistance MOSFET eliminates the need for an external N-channel MOSFET. Aiming at devices requiring accurate overvoltage protection, the protectors suit cell phones, media players, PDAs, and other portable-system applications. Integrated thermal-shutdown protection prevents overcurrent damage, providing ±15-kV ESD protection when bypassing the input with a 1-μF capacitor to ground. Available in a lead-free, 2×2-mm TDFN-8 package, the MAX14527 and the MAX14528 overvoltage protectors cost 90 cents (1000).

Maxim Integrated Products, www.maxim-ic.com

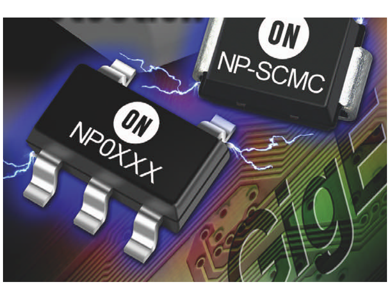
Power-distribution switches have high accuracy

The constant-current TPS2552/3 and latch-off TPS2552-1/3-1 pow-

er-distribution switches handle heavy capacitive loads and prevent short circuits in applications such as USB ports/hubs, cell phones, and laptops. Features include a ±6% current-limit accuracy at 1.3A, a 2.5 to 6.5V input range, and a 75-mA to 1.3A programmable-current-limit threshold using an external resistor with a 6% accuracy. The devices attain a safe output current by switching into a constant-current mode when the output load exceeds the current-limit threshold; the TPS2552-1/3-1 turns the switch off during overcurrent events. The devices find use in simple circuit-breaking or current-limiting applications. Available in SOT23-6 and SON-6 packages, the TPS2552/3 power-distribution switches cost 75 cents (1000).
Texas Instruments, **www.ti.com**

Thyristor-surge-protection devices have low capacitance

Protecting DSL chip sets and line drivers, the NP0080, NP0120, and NP0160 TSPD (thyristor-surge-protection-device) family provides circuit protection during surge and electrostatic-discharge events. Preventing signal distortion on the high-speed data line, the protection devices provide a 3-pF capacitance over operating-voltage ranges. Features include a 50A current-withstanding capability during an 8×20-μsec surge event, and the devices provide tertiary protection between the DSL-isolation transformer and the DSL-line driver in access and customer-premises equipment. The vendor's TSPD family includes the NP-MC series. The NP-MC offers 30-pF capacitance for a 100A-rated device, providing an alternative to gas-discharge tubes in high-speed applications. Available in TSOP-5 packages, the NP0080, NP0120, and NP0160 TSPD cost 23.07 cents (3000); the NP-MC series comes in SMB packaging and costs 23.07 cents (2500).
On Semiconductor,
www.onsemi.com



Transient-suppression module meets avionics, military specifications

A new member of the vendor's COTS standard product line, the VPTi10-28 EMI-filter and voltage-transient-protection module meets avionics and military standards. Combining two modules in a mini package reduces the reflected noise of dc/dc converters and protects the power system from inrush-current damage. The module has an 80V transient operation per military standard 704 and a 100V transient operation per military standard 1275. Additional features include 10A output current, 150W output power, and 45-dB minimum attenuation at 500 kHz. Operating over a −55 to +100°C operating temperature, the VPTi10-28 EMI-filter and voltage-transient-protection module costs $248.33.
VPT, **www.vpt-inc.com**

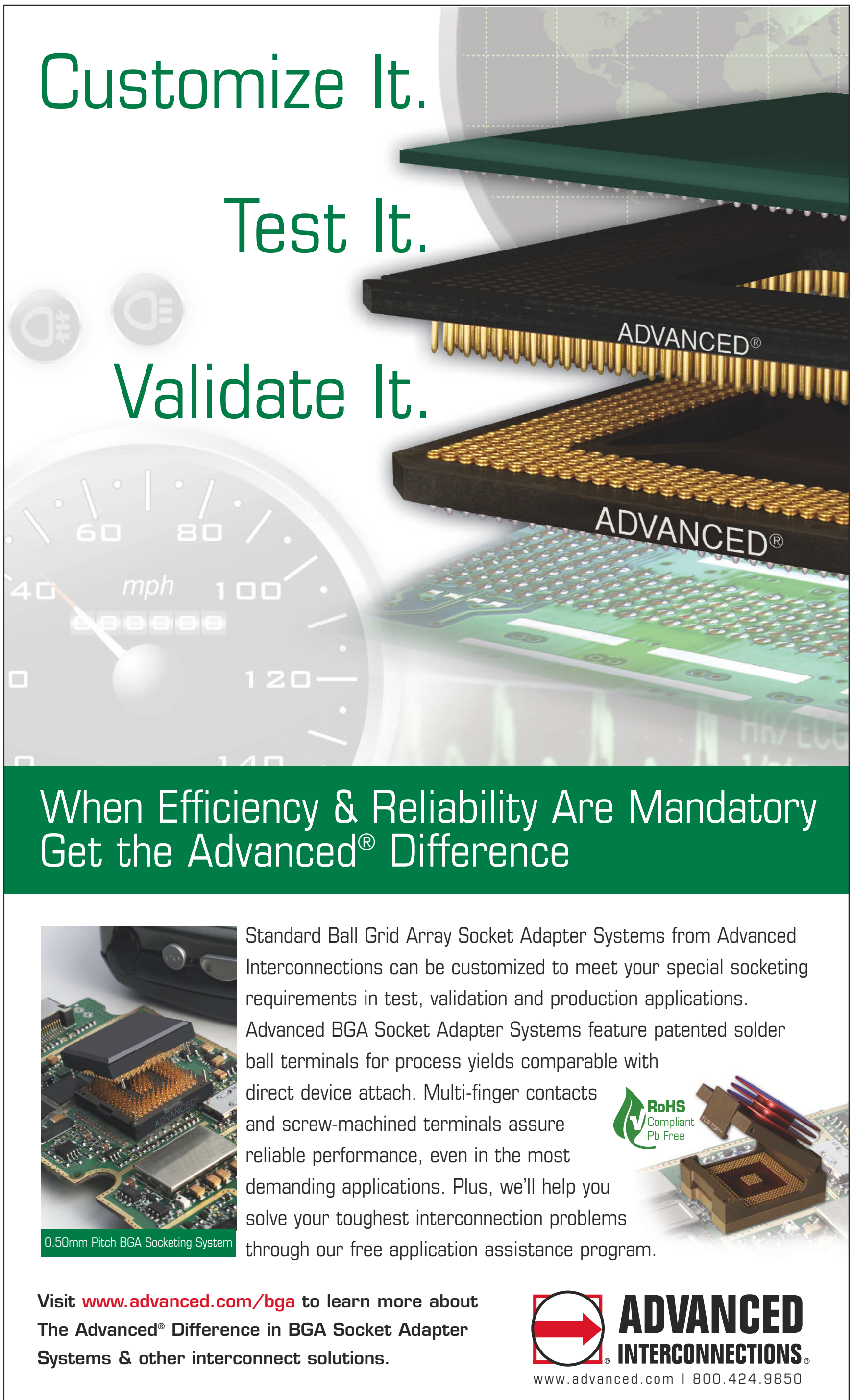
Diode array protects RF antennas from ESD events

Targeting use in RF antennas and portable battery-powered consumer electronics, the OC1214-

CIRCUIT PROTECTION

01TR miniature diode array protects wireless devices using ICs manufactured with submicron technologies that are susceptible to ESD events through the antenna. Combining five diodes, the array allows for a safe dissipation of ±8-kV ESD contact discharge, meeting the IEC 61000-4-2 international standard. The device has a 1-pF input capacitance, preventing signal degradation for the high-speed lines. The protection diodes target applications requiring signal swing above and below ground with a ±7V maximum working voltage. The device also features a leakage current as low as 0.1-µA at 5V. Available in a miniature SOT23-3 package, the OC1214-01TR diode array costs 9 cents.

OnChip Devices, www.onchip.com



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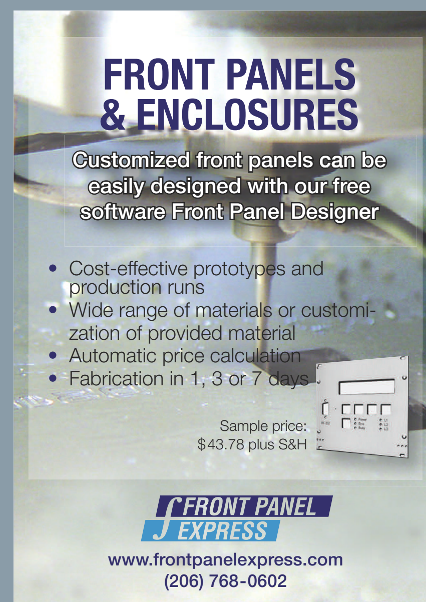

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 BY BOB MASON • SCHNEIDER ELECTRIC

Mismating mix-up makes for monstrous military mission

DANIEL VASCONCELLOS

My first job out of college was for a military-electronics company. We built rectangular metal boxes full of electronics that go into aircraft and space vehicles. Both plug and socket types of keyed circular connectors covered the boxes. We knew that bad things could happen if we mismated the connectors, so we went to great lengths to make sure to plug together only those connectors that were intended for each other. We varied the sizes of the shells and also varied whether a given connector was a plug or a socket. We avoided having two plugs or sockets of the same diameter. If we absolutely had to have two shells of the same size and type, we made sure that each one had unique keying configurations that were incompatible with any other connectors on the box.

So, in accordance with Murphy's law, an aircraft-maintenance technician somehow managed to mate two plug-type connectors together, despite all of the size, keying, and other preventive measures that we had designed in. The result of this configuration was a large flash and loud boom when he powered up the aircraft. The electronics unit was destroyed, as were other circuits in the aircraft.

Although we were impressed with the technician's ingenuity and perseverance, the officers in his chain of command were not amused. The general in charge of the air base got directly involved.

He first ordered us to determine what would occur if *any* connector signal on the box were to be connected to *any other* connector signal on the box, regardless of whether it was physically possible. After determining that outcome, he instructed us to make whatever circuit changes were necessary to make such a mismating innocuous. He didn't go as far as to tell us to make it work in that configuration, but he did insist that no damage occur.

Our managers, duly chastened after their visit to the general's office, immediately set to work. They put together a task force to start the cross-connection analysis. The task facing us was enormous. The box had 20 connectors, each with about 30 pins. When we began, it took several hours to analyze the effect of shorting a pair of signals together. As we got used to the work, that time dropped to about one hour per pair. This phase was only for analysis, however; it didn't include redesign. After several days, we saw how little progress we were making. We decided to determine the scope of the task.

The math wasn't hard: 20 connectors of 30 pins each totals 600 pins. The combination of 600 items, two at a time, is 179,700 combinations. At an hour each, that job would take 179,700 man-hours, or 86.4 man-years. The four people on the team could count on spending the next 21+ years doing these analyses.

We presented our figures to our management. They didn't say much, but we saw some eyebrows rise. Management took our figures to the general. We never heard what the general said, but the next week we were taken off the connector analysis and returned to our interrupted projects.

The lessons I learned from this experience were that you should always define the scope of a job in the beginning, and, whenever you think you have made something idiot-proof, remember, along will come a better idiot. EDN

Bob Mason is a staff electronics engineer at Schneider Electric. You can reach him at bob.mason@us.schneider-electric.com.

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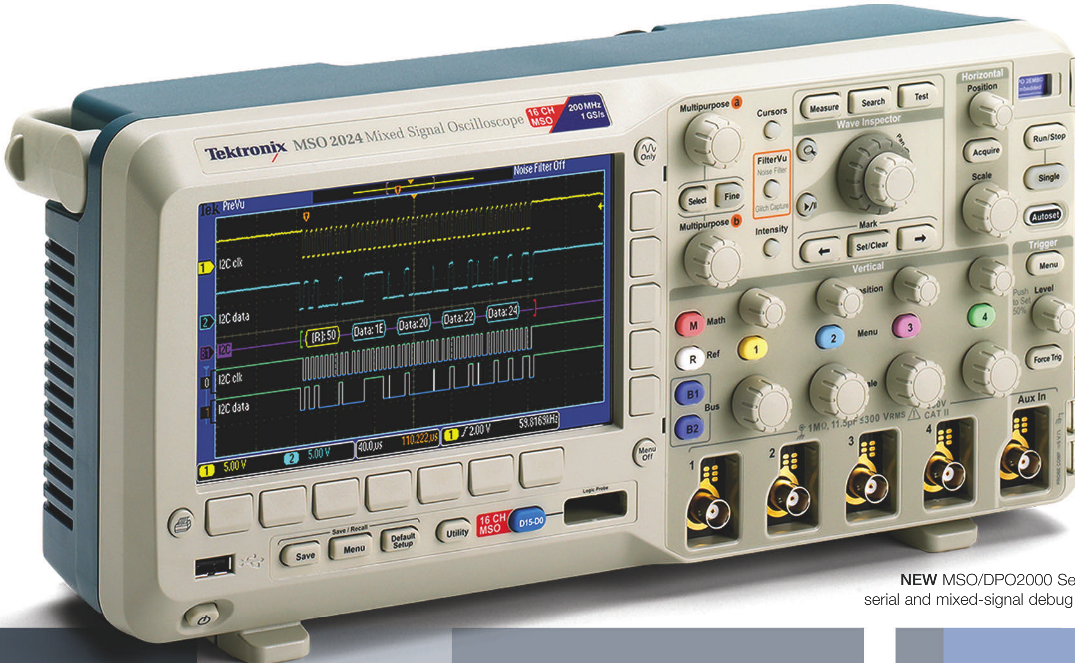

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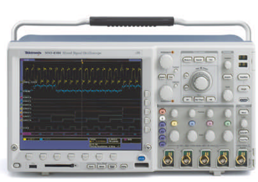

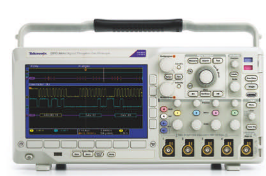

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